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UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

WESTERN DIVISION

PEREGRINE SEMICONDUCTOR CORPORATION, a Delaware corporation,

Plaintiff,

vs.

RF MICRO DEVICES, INC., a North Carolina corporation, MOTOROLA MOBILITY, INC., a Delaware corporation, and JOHN DOES 1-10,

Defendants.

CASE NO. **SACV12-248 JST(RNBx)**

COMPLAINT FOR DAMAGES AND INJUNCTIVE RELIEF

(1) Patent Infringement under 35 U.S.C. §§ 271, 281, 283-85

DEMAND FOR JURY TRIAL

For its complaint against Defendants RF Micro Devices, Inc. ("RFMD"), Motorola Mobility, Inc. ("MMI"), and John Does 1-10 (collectively, "Defendants"), Plaintiff Peregrine Semiconductor Corporation ("Peregrine") complains and alleges as follows:

NATURE OF ACTION

This is an action for patent infringement arising under the patent laws of the United States, Title 35 of the United States Code. Plaintiff seeks damages, attorneys' fees, costs, and preliminary and permanent injunctive relief.

JURISDICTION

1. This Court has subject matter jurisdiction over this case pursuant to 28 U.S.C. § 1338(a).

2. This Court has personal jurisdiction over Defendant RFMD based upon the following: (a) Defendant RFMD maintains an office in the Central District of California; (b) Defendant RFMD transacts substantial business in and maintains continuous and systematic contacts with this District and the State of California; and (c) Defendant RFMD has committed tortious acts that RFMD knew or should have known would cause injury to Plaintiff in the State of California.

3. This Court has personal jurisdiction over Defendant MMI based upon the following: (a) Defendant MMI transacts substantial business in and maintains continuous and systematic contacts with this District and the State of California; (b) Defendant MMI maintains offices in the State of California, (c) Defendant MMI has committed tortious acts that MMI knew or should have known would cause injury to Plaintiff in the State of California, and (d) Defendant MMI has appointed an agent in this District to receive service of process.

4. This Court has personal jurisdiction over Defendants John Does 1-10 based on the following: (a) Defendants John Does 1-10 are present and/or doing business in the Central District of California; and (b) Defendants John Does 1-10 have committed tortious acts that they knew or should have known would cause injury to Plaintiff in the State of California.

5. Venue is proper in the United States District Court for the Central District of California under 28 U.S.C. §§ 1391(b), 1400(b).

PARTIES

6. Plaintiff Peregrine is a Delaware corporation with a principal place of business at 9380 Carroll Park Drive, San Diego, California 92121.

7. Upon information and belief, Defendant RFMD is a North Carolina corporation with a principal place of business at 7628 Thorndike Road, Greensboro, North Carolina 27409.

8. Upon information and belief, Defendant MMI is a Delaware corporation with a principal place of business at 600 N. US Hwy 45, Libertyville, Illinois 60048.

9. Defendants John Does 1-10 are parties whose identities are not yet known to Peregrine. To the extent their identities become known to Plaintiff Peregrine, the John Doe defendants will be named and their activities pleaded in an amended complaint.

FACTUAL ALLEGATIONS

Plaintiff Peregrine is the owner by assignment of all rights, title, and interest in and to United States Patent Nos. 7,910,993 (the "'993 Patent"), 7,123,898 (the "'898 Patent"), 7,460,852 (the "'852 Patent"), 7,796,969 (the "'969 Patent"), and 7,860,499 (the "'499 Patent") (collectively, the "Peregrine Patents") (Exhibits A-E). The '993 Patent is entitled "Method and Apparatus for Use in Improving Linearity of MOSFET's Using an Accumulated Charge Sink" and issued March 22, 2011. The '898 Patent is entitled "Switch Circuit and Method of Switching Radio Frequency Signals" and issued October 17, 2006. The '852 Patent is entitled "Switch Circuit and Method of Switching Radio Frequency Signals" and issued December 2, 2008. The '969 Patent is entitled "Symmetrically and Asymmetrically Stacked Transistor Group RF Switch" and issued September 14, 2010. Lastly, the '499 Patent is entitled "Switch Circuit and Method of Switching Radio Frequency Signals" and issued December 28, 2010. Accordingly, Peregrine has standing to sue for infringement of the Asserted Patents.

The Asserted Patents disclose advanced integrated circuit technologies for use in

radio frequency circuits, including but not limited to radio frequency switches. Radio frequency circuits practicing the Asserted Patents can be used in a variety of devices including, for example, antenna tuning circuits, devices that use diversity or multiple-input and multiple-output (MMO) antennas, and mobile wireless devices that use cellular technologies and wireless local area network (WLAN) technologies. Mobile wireless devices that use radio frequency circuits practicing the Asserted Patents may (a) transmit and/or receive wireless signals more efficiently while consuming less power, (b) be smaller in size because the Asserted Patents disclose techniques that allow the integration of functions that previously had to be handled by separate components, and (c) be less expensive to manufacture due to the ability to leverage the established global Complimentary Metal Oxide Semiconductor ("CMOS") manufacturing infrastructure, rather than needing to rely on the more specialized manufacturing processes required by the devices that utilized previously available technologies and techniques. After significant investments in research and development, engineering, labor, plant and equipment, manufacturing and marketing, Peregrine-branded radio frequency switches that practice the Asserted Patents have been selected for use in wireless handsets by many of the leading wireless handset manufacturers including Apple, LG, Nokia, Samsung, and Sony Ericsson.

Upon information and belief, RFMD has and continues to infringe, contributorily infringe, and/or induce infringement of the Asserted Patents by knowingly and actively (1) making, having made, importing, using, offering for sale and/or selling products that infringe one or more claims of the Asserted Patents, including integrated circuits with integrated circuit die markings M1D1604 and M1D1293 such as RF1603, RF1604, and RF1293, (2) inducing others to do the same, and (3) contributing to the manufacture, import, use, sale, or offer for sale products that infringe one or more claims of the Asserted Patents. In addition, upon information and belief, MMI has and continues to infringe, contributorily infringe, and/or induce infringement of the Asserted Patents by knowingly and actively (1) making, having made, importing, using, offering for sale

and/or selling products that infringe one or more claims of the Asserted Patents, including MMI's DROID RAZR and DROID BIONIC handsets (Model Nos. XT912 and XT875, respectively), both of which contain RF1603, which contains integrated circuit die marking M1D1604, (2) inducing others to do the same, and (3) contributing to the manufacture, import, use, sale, or offer for sale products that infringe one or more claims of the Asserted Patents. The RF1603, RF1604, RF1293, DROID RAZR handset, and DROID BIONIC handset infringe at least claims 14-16 and 23-25 of the '993 Patent, claims 1-3, 5-7, and 15 of the '898 Patent, claims 1-4, 7, 13, 14, 20, 22, 24, and 25 of the '852 Patent, claims 6-8 and 29-30 of the '969 Patent, and claims 1, 3, 5 and 6 of the '499 Patent.

FIRST CAUSE OF ACTION

(Infringement of the '993 Patent)

10. Plaintiff incorporates the allegations in the preceding paragraphs as if fully set forth herein.

11. Plaintiff Peregrine is the owner by assignment of all rights, title, and interest in and to the '993 Patent. Peregrine therefore has standing to sue for infringement of the '993 Patent.

12. Upon information and belief, Defendants have infringed and continue to infringe the '993 Patent by knowingly and actively making, having made, importing, using, offering to sell, or selling products that infringe one or more claims of the '993 Patent, including but not limited to certain integrated circuits (including those with integrated circuit die markings M1D1604 and M1D1293 such as RF1603, RF1604, and RF1293, which are marketed and sold by RFMD), components thereof, and/or devices using certain integrated circuits or components thereof (such as MMI's DROID RAZR and DROID BIONIC handsets, which are marketed and sold by MMI) that incorporate, without license, the inventions developed by Peregrine and protected by one or more claims in the '993 Patent, or by knowingly and actively inducing or contributing to the infringement of the '993 Patent by others.

13. Plaintiff Peregrine has complied with 35 U.S.C. § 287.

14. As a direct and proximate result of Defendants' infringement, Plaintiff Peregrine has suffered, and will continue to suffer, injury.

15. As a result of the harm suffered as alleged herein, Plaintiff Peregrine is entitled to all of the remedies available under the Patent Act, including damages adequate to compensate it for such infringement, but in no event less than a reasonable royalty, costs and attorneys' fees.

SECOND CAUSE OF ACTION

(Infringement of the '898 Patent)

16. Plaintiff incorporates the allegations in the preceding paragraphs as if fully set forth herein.

17. Plaintiff Peregrine is the owner by assignment of all rights, title, and interest in and to the '898 Patent. Peregrine therefore has standing to sue for infringement of the '898 Patent.

18. Upon information and belief, Defendants have infringed and continue to infringe the '898 Patent by knowingly and actively making, having made, importing, using, offering to sell, or selling products that infringe one or more claims of the '898 Patent, including but not limited to certain integrated circuits (including those with integrated circuit die markings M1D1604 and M1D1293 such as RF1603, RF1604, and RF1293, which are marketed and sold by RFMD), components thereof, and/or devices using certain integrated circuits or components thereof (such as MMI's DROID RAZR and DROID BIONIC handsets, which are marketed and sold by MMI) that incorporate, without license, the inventions developed by Peregrine and protected by one or more claims in the '898 Patent, or by knowingly and actively inducing or contributing to the infringement of the '898 Patent by others.

19. Plaintiff Peregrine has complied with 35 U.S.C. § 287.

20. As a direct and proximate result of Defendants' infringement, Plaintiff Peregrine has suffered, and will continue to suffer, injury.

21. As a result of the harm suffered as alleged herein, Plaintiff Peregrine is entitled to all of the remedies available under the Patent Act, including damages adequate to compensate it for such infringement, but in no event less than a reasonable royalty, costs and attorneys' fees.

THIRD CAUSE OF ACTION

(Infringement of the '852 Patent)

22. Plaintiff incorporates the allegations in the preceding paragraphs as if fully set forth herein.

23. Plaintiff Peregrine is the owner by assignment of all rights, title, and interest in and to the '852 Patent. Peregrine therefore has standing to sue for infringement of the '852 Patent.

24. Upon information and belief, Defendants have infringed and continue to infringe the '852 Patent by knowingly and actively making, having made, importing, using, offering to sell, or selling products that infringe one or more claims of the '852 Patent, including but not limited to certain integrated circuits (including those with integrated circuit die markings M1D1604 and M1D1293 such as RF1603, RF1604, and RF1293, which are marketed and sold by RFMD), components thereof, and/or devices using certain integrated circuits or components thereof (such as MMI's DROID RAZR and DROID BIONIC handsets, which are marketed and sold by MMI) that incorporate, without license, the inventions developed by Peregrine and protected by one or more claims in the '852 Patent, or by knowingly and actively inducing or contributing to the infringement of the '852 Patent by others.

25. Plaintiff Peregrine has complied with 35 U.S.C. § 287.

26. As a direct and proximate result of Defendants' infringement, Plaintiff Peregrine has suffered, and will continue to suffer, injury.

27. As a result of the harm suffered as alleged herein, Plaintiff Peregrine is entitled to all of the remedies available under the Patent Act, including damages adequate to compensate it for such infringement, but in no event less than a reasonable royalty,

costs and attorneys' fees.

FOURTH CAUSE OF ACTION

(Infringement of the '969 Patent)

28. Plaintiff incorporates the allegations in the preceding paragraphs as if fully set forth herein.

29. Plaintiff Peregrine is the owner by assignment of all rights, title, and interest in and to the '969 Patent. Peregrine therefore has standing to sue for infringement of the '969 Patent.

30. Upon information and belief, Defendants have infringed and continue to infringe the '969 Patent by knowingly and actively making, having made, importing, using, offering to sell, or selling products that infringe one or more claims of the '969 Patent, including but not limited to certain integrated circuits (including those with integrated circuit die markings M1D1604 and M1D1293 such as RF1603, RF1604, and RF1293, which are marketed and sold by RFMD), components thereof, and/or devices using certain integrated circuits or components thereof (such as MMI's DROID RAZR and DROID BIONIC handsets, which are marketed and sold by MMI) that incorporate, without license, the inventions developed by Peregrine and protected by one or more claims in the '969 Patent, or by knowingly and actively inducing or contributing to the infringement of the '969 Patent by others.

31. Plaintiff Peregrine has complied with 35 U.S.C. § 287.

32. As a direct and proximate result of Defendants' infringement, Plaintiff Peregrine has suffered, and will continue to suffer, injury.

33. As a result of the harm suffered as alleged herein, Plaintiff Peregrine is entitled to all of the remedies available under the Patent Act, including damages adequate to compensate it for such infringement, but in no event less than a reasonable royalty, costs and attorneys' fees.

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FIFTH CAUSE OF ACTION

(Infringement of the '499 Patent)

34. Plaintiff incorporates the allegations in the preceding paragraphs as if fully set forth herein.

35. Plaintiff Peregrine is the owner by assignment of all rights, title, and interest in and to the '499 Patent. Peregrine therefore has standing to sue for infringement of the '499 Patent.

36. Upon information and belief, Defendants have infringed and continue to infringe the '499 Patent by knowingly and actively making, having made, importing, using, offering to sell, or selling products that infringe one or more claims of the '499 Patent, including but not limited to certain integrated circuits (including those with integrated circuit die markings M1D1604 and M1D1293 such as RF1603, RF1604, and RF1293, which are marketed and sold by RFMD), components thereof, and/or devices using certain integrated circuits or components thereof (such as MMI's DROID RAZR and DROID BIONIC handsets, which are marketed and sold by MMI) that incorporate, without license, the inventions developed by Peregrine and protected by one or more claims in the '499 Patent, or by knowingly and actively inducing or contributing to the infringement of the '499 Patent by others.

37. Plaintiff Peregrine has complied with 35 U.S.C. § 287.

38. As a direct and proximate result of Defendants' infringement, Plaintiff Peregrine has suffered, and will continue to suffer, injury.

39. As a result of the harm suffered as alleged herein, Plaintiff Peregrine is entitled to all of the remedies available under the Patent Act, including damages adequate to compensate it for such infringement, but in no event less than a reasonable royalty, costs and attorneys' fees.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff Peregrine respectfully prays that the Court grant the following relief:

A. The entry of judgment in favor of Plaintiff Peregrine and against the Defendants;

B. A preliminary and permanent injunction prohibiting the Defendants, their respective officers, agents, servants, employees and/or all persons acting in concert or participation with them, or any of them, from engaging in further infringement and/or acts of infringement and inducement of the Peregrine Patent;

C. An award of damages adequate to compensate Plaintiff Peregrine for the infringement, as well as prejudgment interest from the date the infringement began, but in no event less than a reasonable royalty as permitted by 35 U.S.C. § 285;

D. A finding that, to the extent the Defendants knew of their infringing activities, the Defendants' infringement was willful;

E. An award of treble damages for the period of any willful infringement pursuant to 35 U.S.C. § 284;

F. A finding that this case is exceptional and an award of interest, costs and attorneys' fees incurred by Plaintiff Peregrine in prosecuting this action as provided by 35 U.S.C. § 285; and

G. For any other orders necessary to accomplish complete justice between the parties; and

H. For such other and further relief as this Court or a jury may deem just and proper.

JURY DEMAND

Plaintiff Peregrine demands a trial by jury on all issues triable by jury.

DATED: February 14, 2012

GREENBERG TRAURIG, LLP

By _____

Allan Z. Litovsky
Michaele N. Turnage Young
Attorneys for Plaintiff,
Peregrine Semiconductor Corporation

Exhibit “A”

U 7337806

THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

January 26, 2012

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THIS OFFICE OF:

U.S. PATENT: *7,910,993*
ISSUE DATE: *March 22, 2011*

By Authority of the
Under Secretary of Commerce for Intellectual Property
and Director of the United States Patent and Trademark Office

P. SWAIN
Certifying Officer

US007910993B2

(12) **United States Patent**
Brindle et al.

(10) **Patent No.: US 7,910,993 B2**
(45) **Date of Patent: Mar. 22, 2011**

(54) **METHOD AND APPARATUS FOR USE IN IMPROVING LINEARITY OF MOSFET'S USING AN ACCUMULATED CHARGE SINK**

(75) Inventors: **Christopher N. Brindle**, Poway, CA (US); **Michael A. Stuber**, Carlsbad, CA (US); **Dylan J. Kelly**, San Diego, CA (US); **Clint L. Kemerling**, Escondido, CA (US); **George P. Imthurn**, San Diego, CA (US); **Robert B. Welstand**, San Diego, CA (US); **Mark L. Burgener**, San Diego, CA (US)

(73) Assignee: **Peregrine Semiconductor Corporation**, San Diego, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 613 days.

(21) Appl. No.: **11/484,370**

(22) Filed: **Jul. 10, 2006**

(65) **Prior Publication Data**

US 2007/0018247 A1 Jan. 25, 2007

Related U.S. Application Data

(60) Provisional application No. 60/698,523, filed on Jul. 11, 2005, provisional application No. 60/718,260, filed on Sep. 15, 2005.

(51) **Int. Cl.**
H01L 27/12 (2006.01)

(52) **U.S. Cl.** **257/347**

(58) **Field of Classification Search** 257/347, 257/59, 61, 333, 346, 327, 40, 402, 403, 257/314–326, 105, 288, 401, 901
See application file for complete search history.

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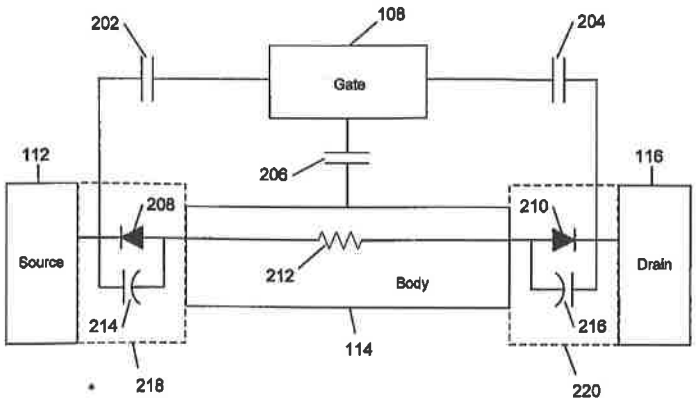
Primary Examiner — Dao H Nguyen
Assistant Examiner — Tram H Nguyen
(74) *Attorney, Agent, or Firm* — Jaquez & Associates; Martin J. Jaquez, Esq.

(57) **ABSTRACT**

A method and apparatus for use in improving the linearity characteristics of MOSFET devices using an accumulated charge sink (ACS) are disclosed. The method and apparatus are adapted to remove, reduce, or otherwise control accumulated charge in SOI MOSFETs, thereby yielding improvements in FET performance characteristics. In one exemplary embodiment, a circuit having at least one SOI MOSFET is configured to operate in an accumulated charge regime. An accumulated charge sink, operatively coupled to the body of the SOI MOSFET, eliminates, removes or otherwise controls accumulated charge when the FET is operated in the accumulated charge regime, thereby reducing the nonlinearity of the parasitic off-state source-to-drain capacitance of the SOI MOSFET. In RF switch circuits implemented with the improved SOI MOSFET devices, harmonic and intermodulation distortion is reduced by removing or otherwise controlling the accumulated charge when the SOI MOSFET operates in an accumulated charge regime.

39 Claims, 22 Drawing Sheets



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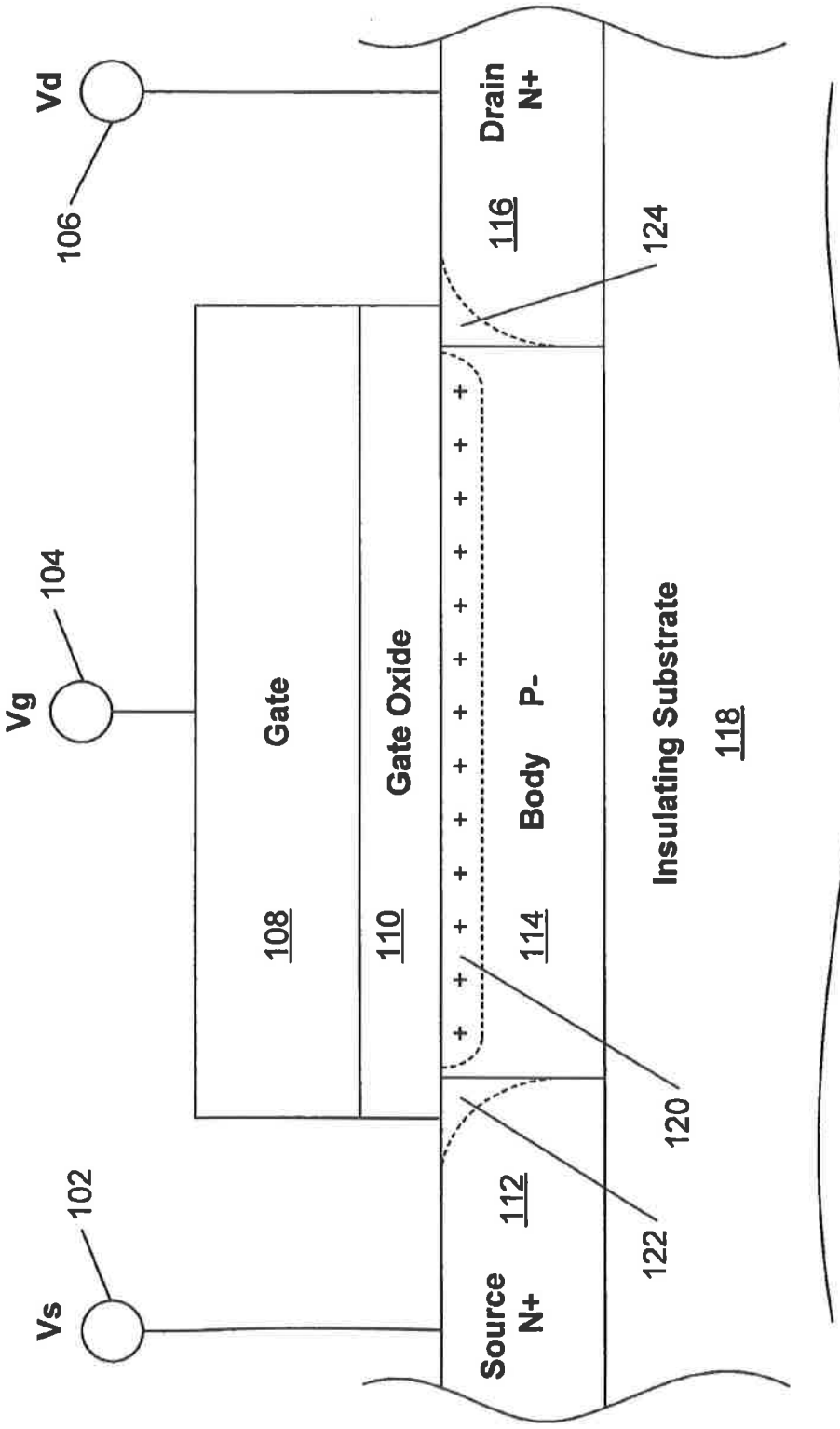


Figure 1 (Prior Art)

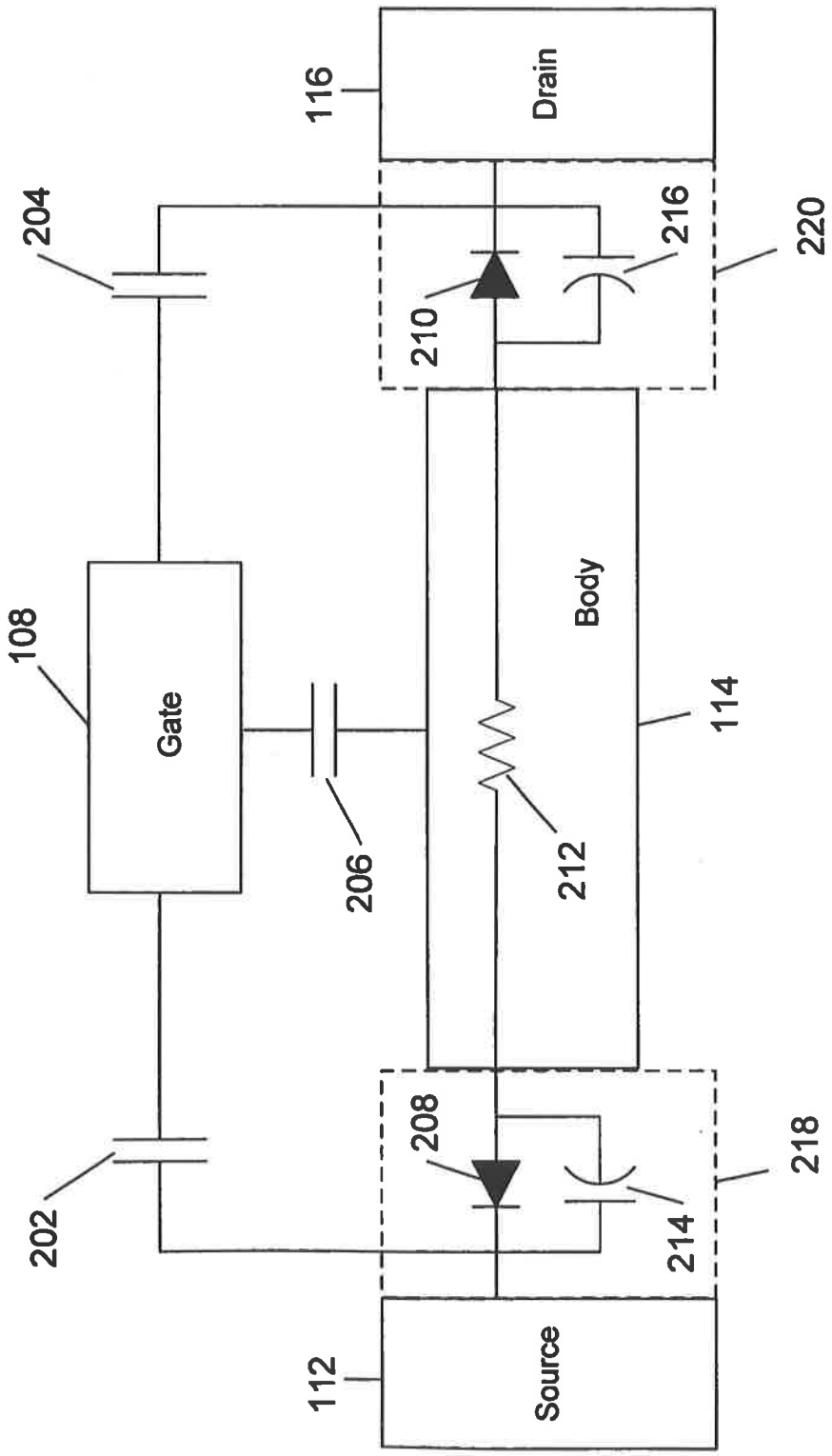


Figure 2A

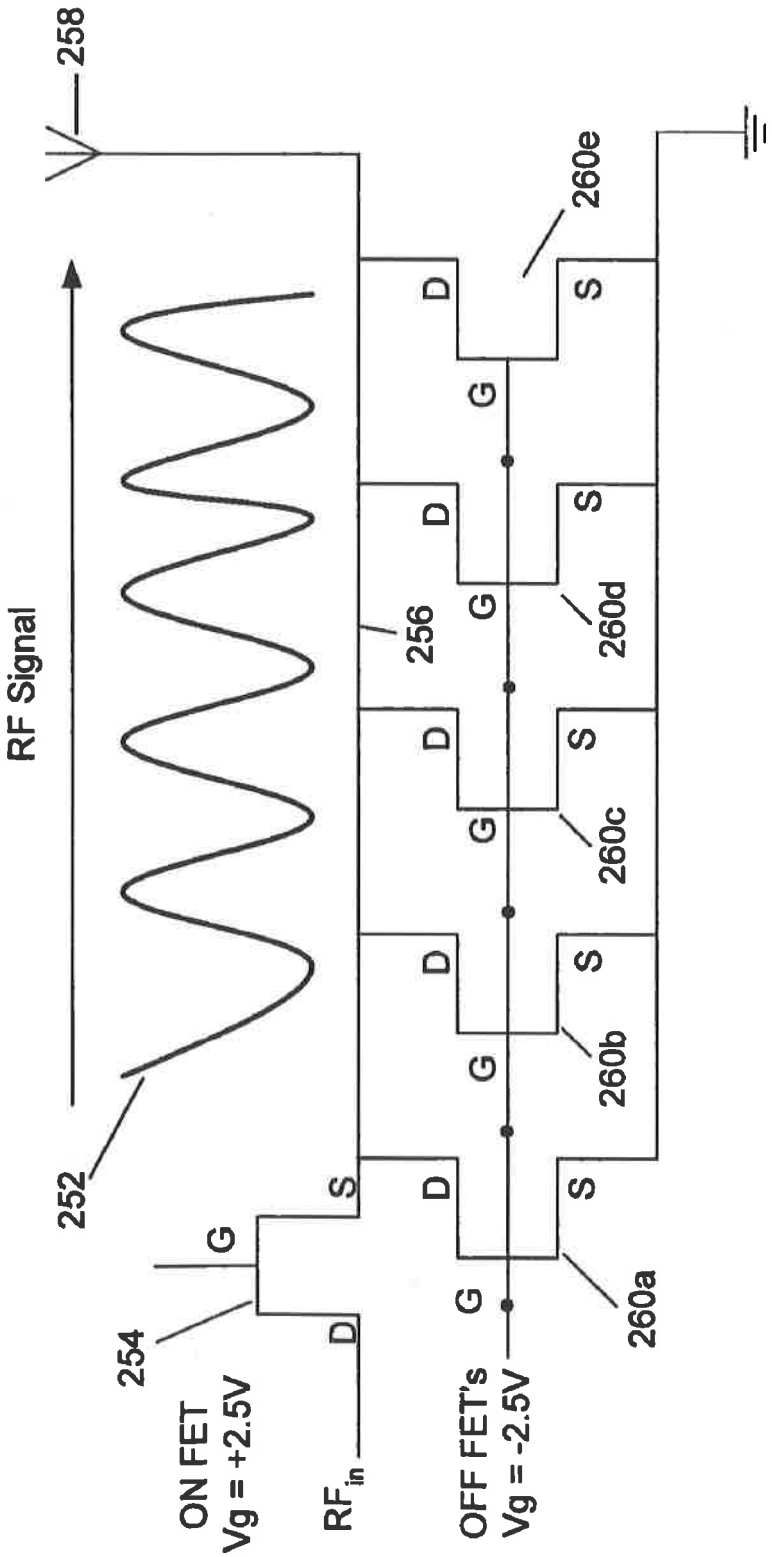


FIGURE 2B

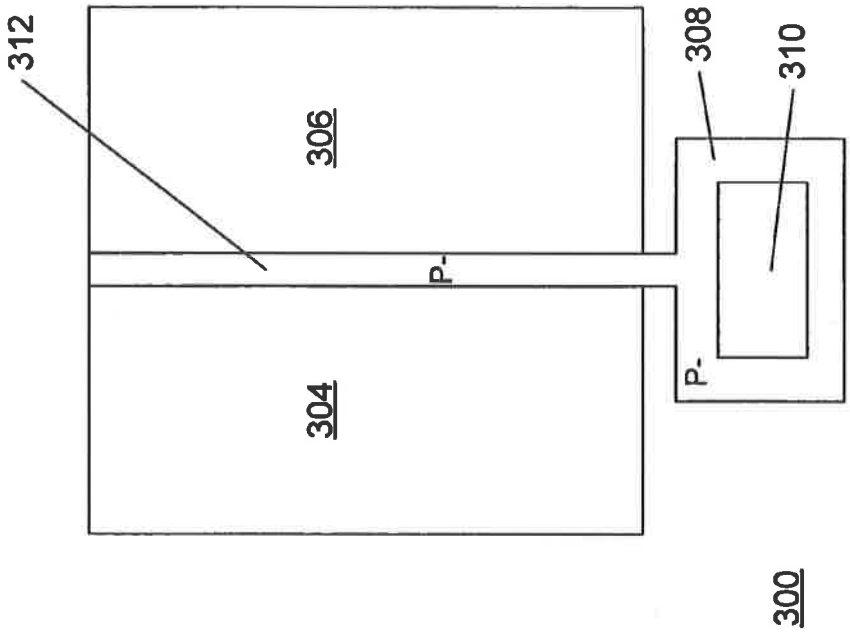
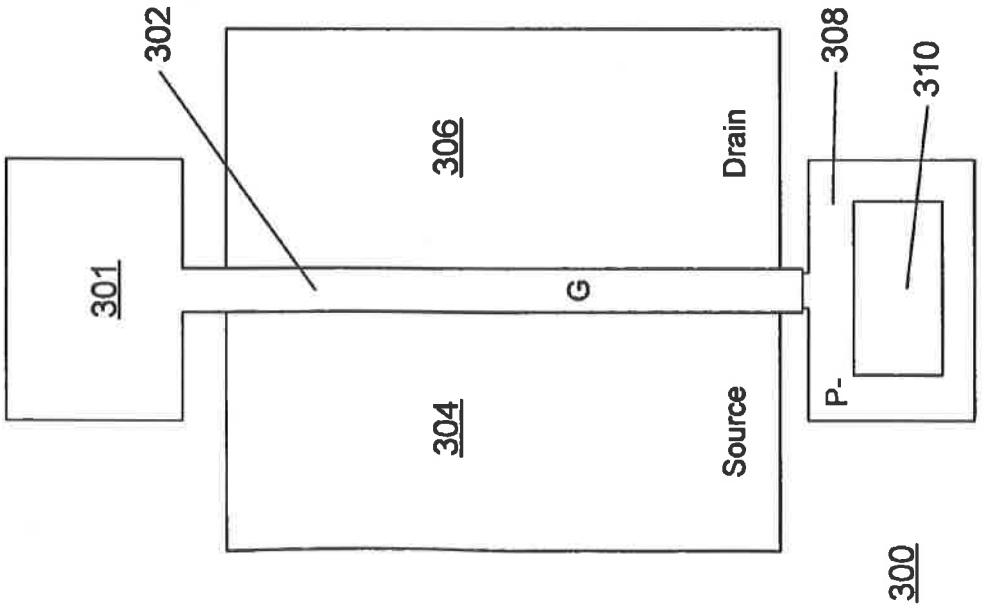


Figure 3B



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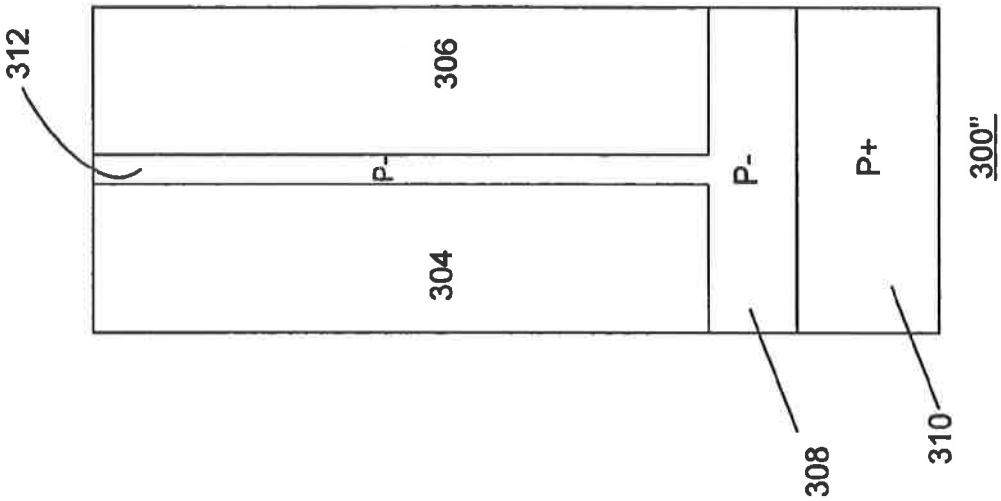


Figure 3D

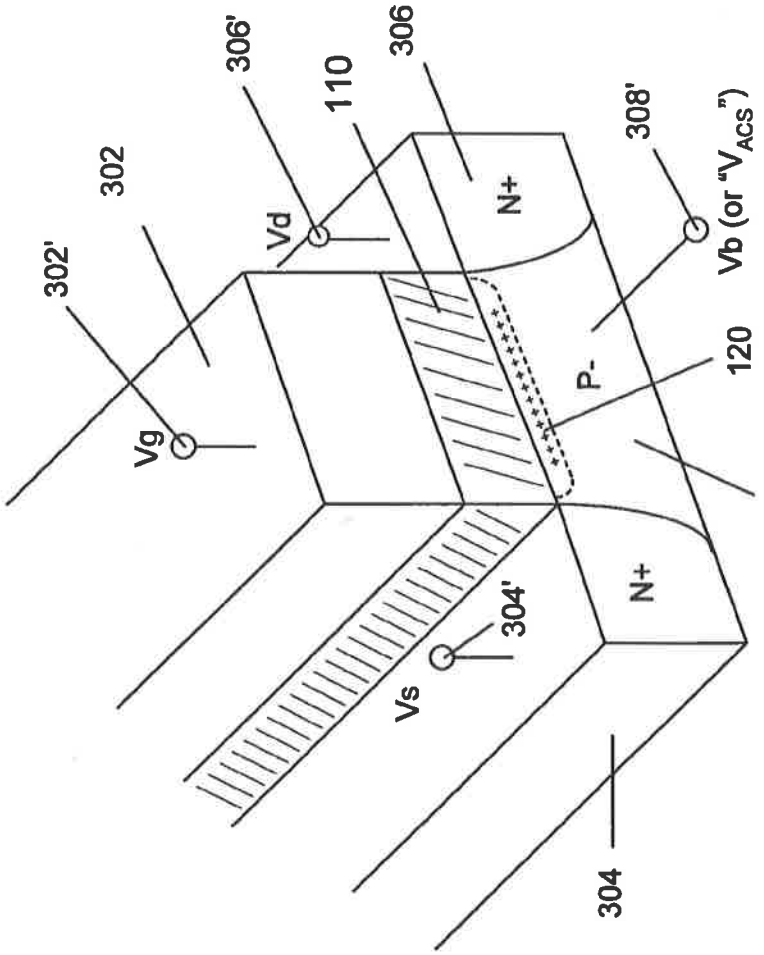
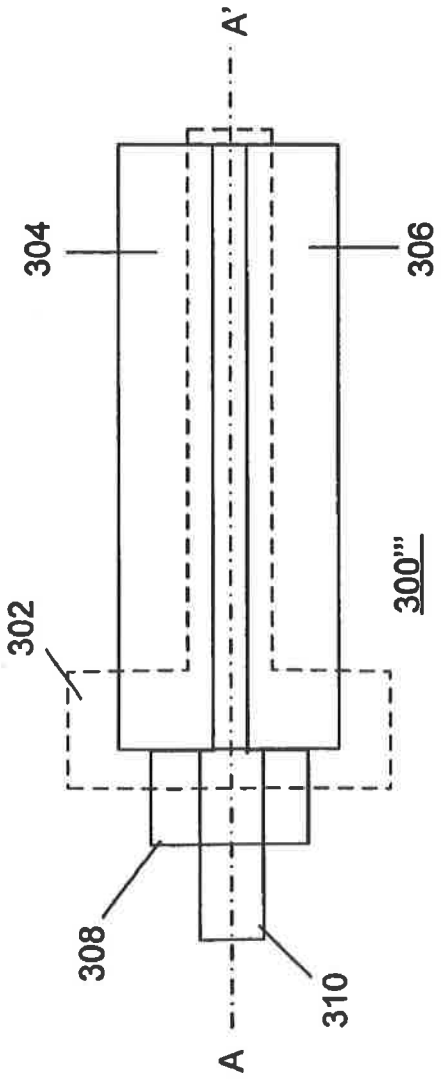


Figure 3C



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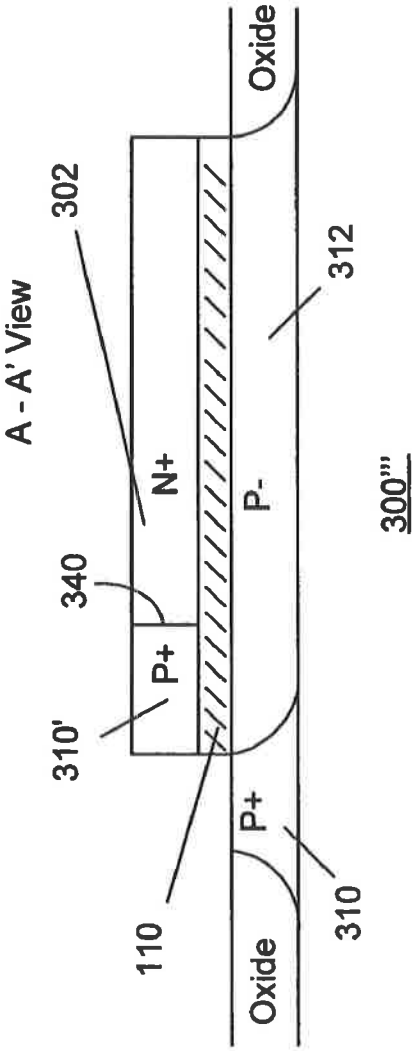

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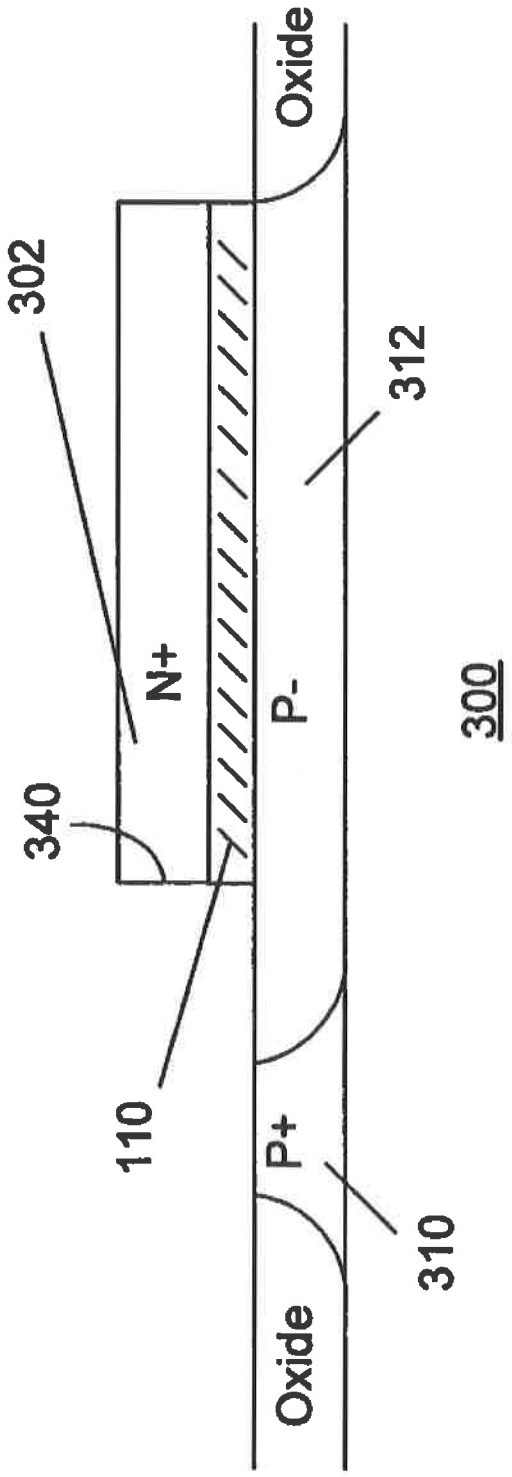
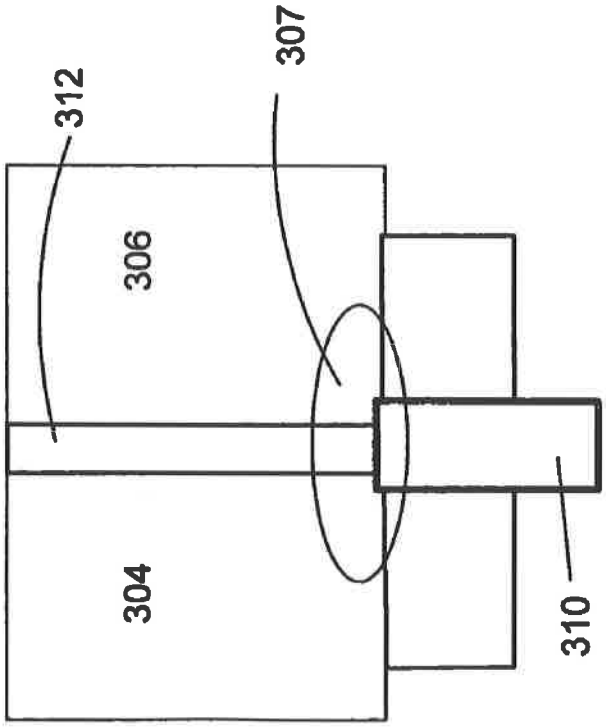


Figure 3G

Figure 3H



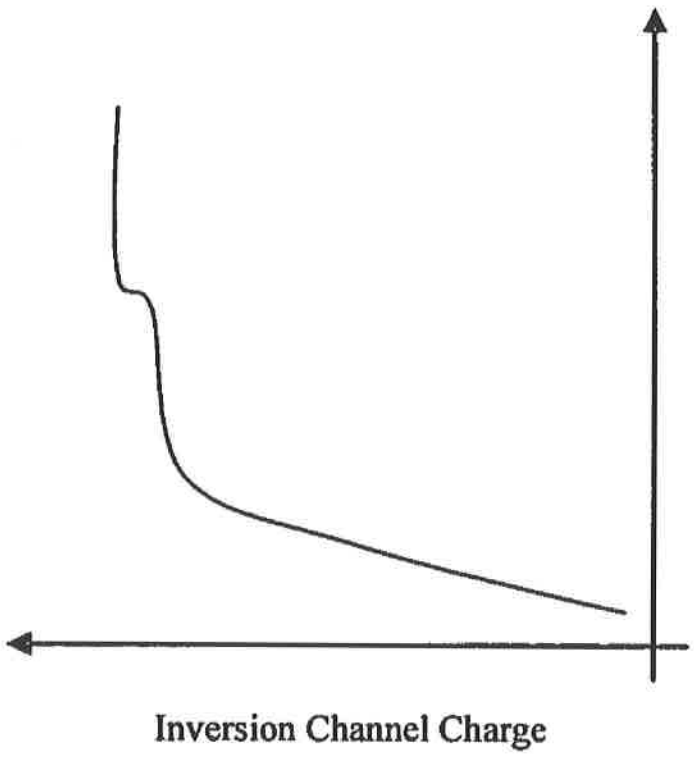


Figure 3I

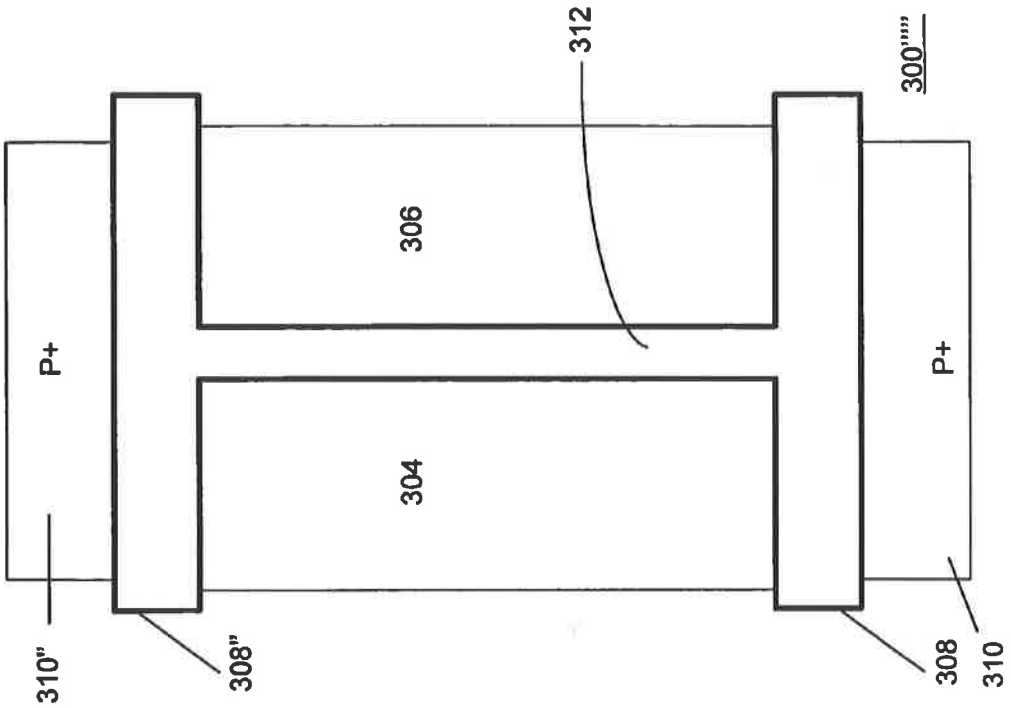
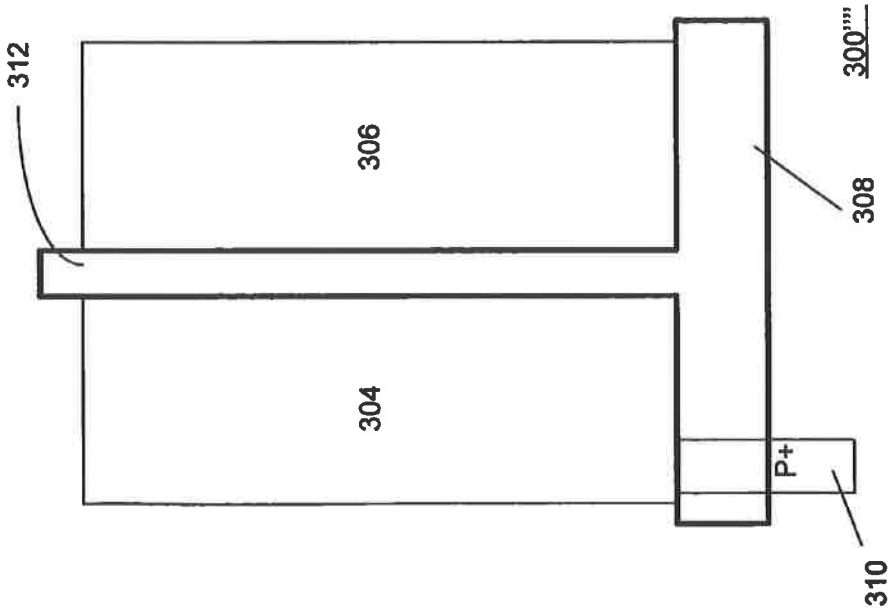


Figure 3K



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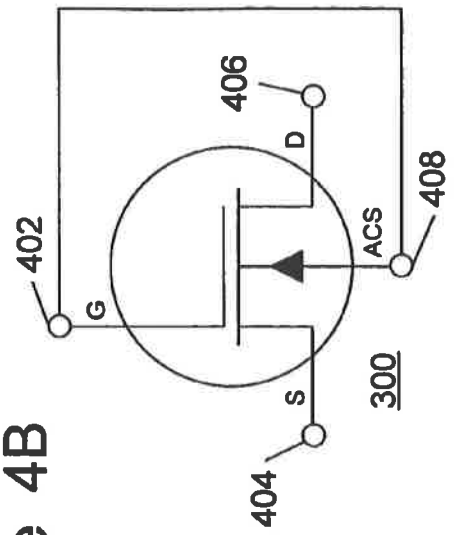
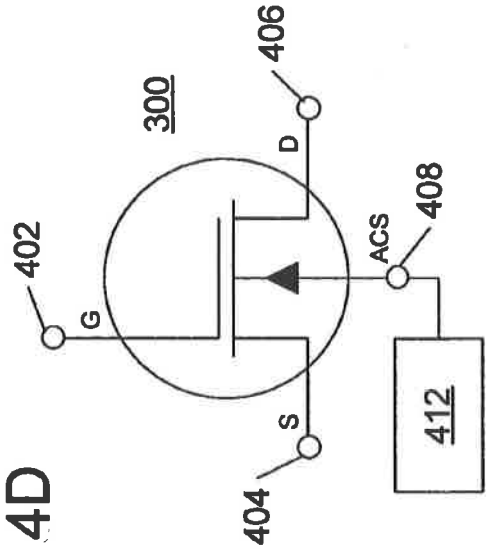


Figure 4B



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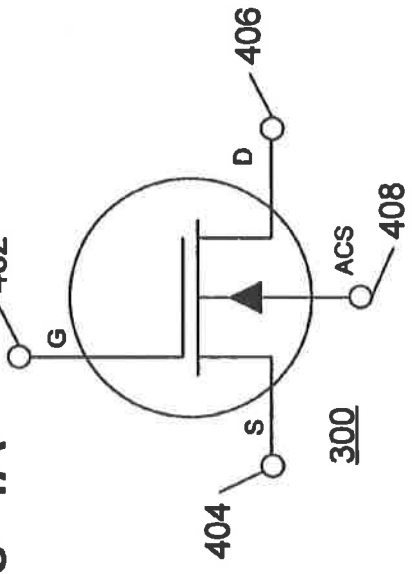


Figure 4A

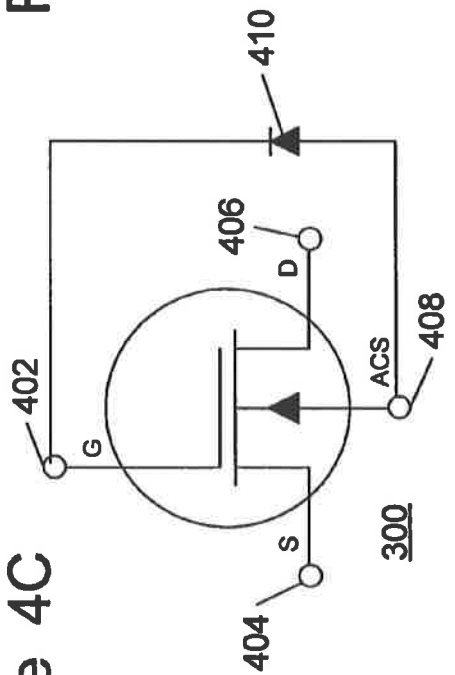
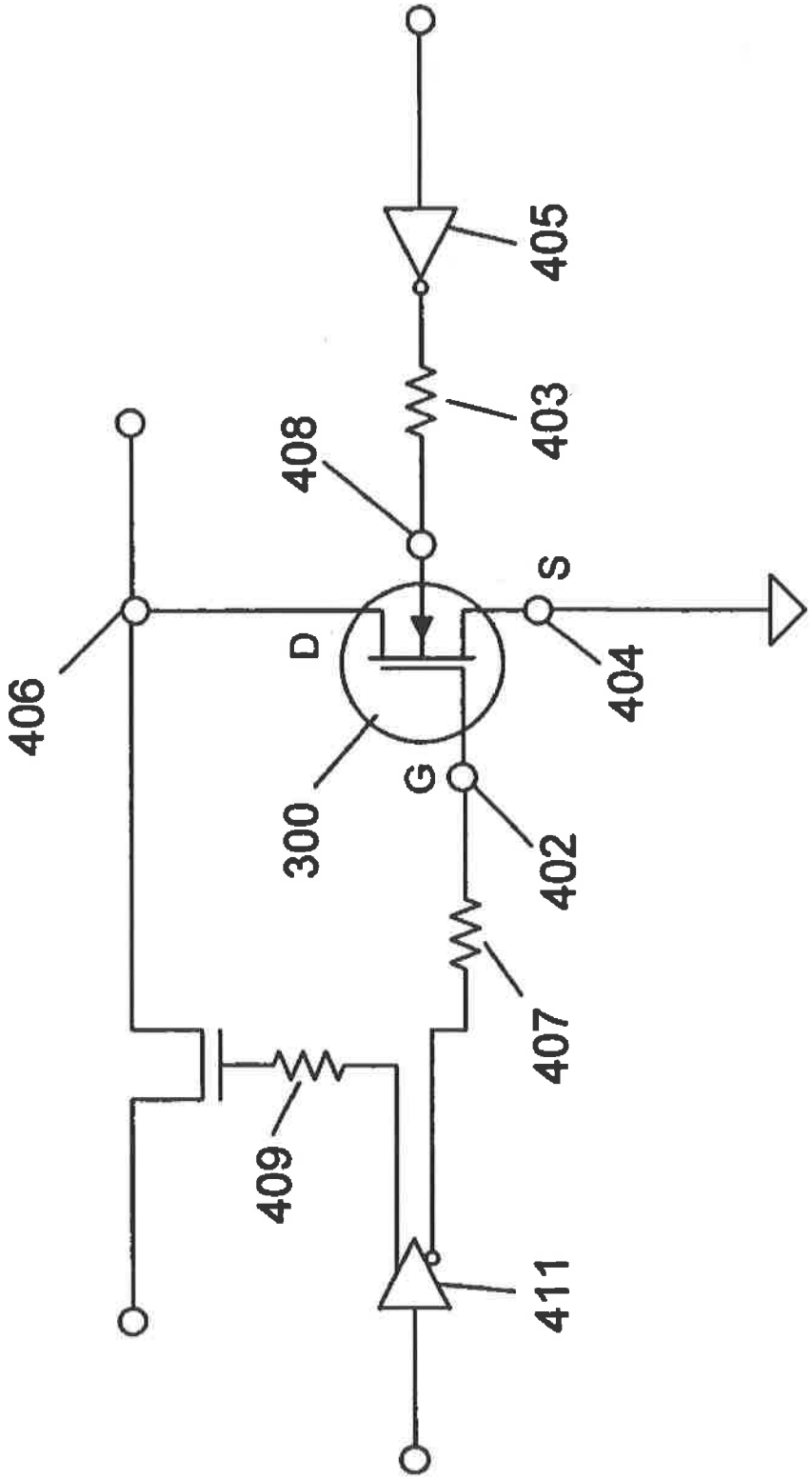


Figure 4C



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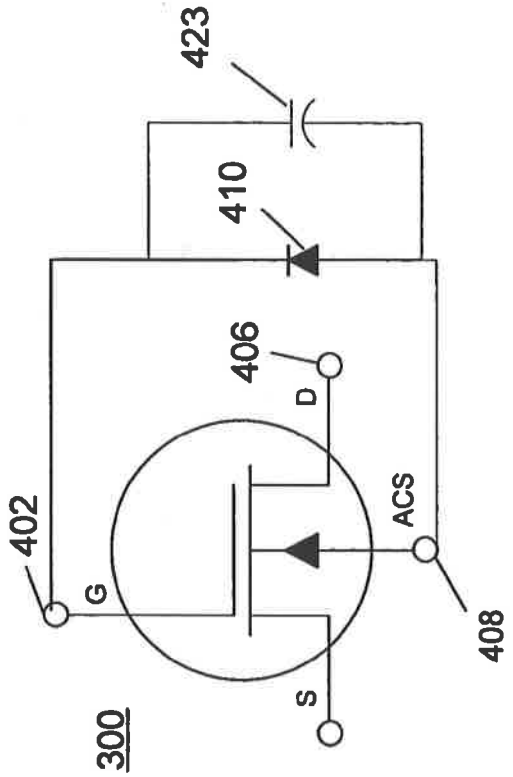

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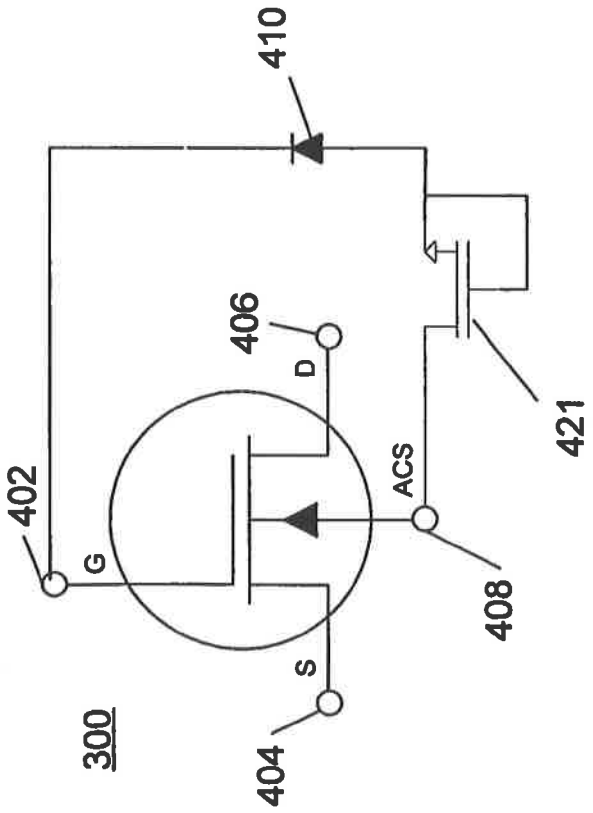

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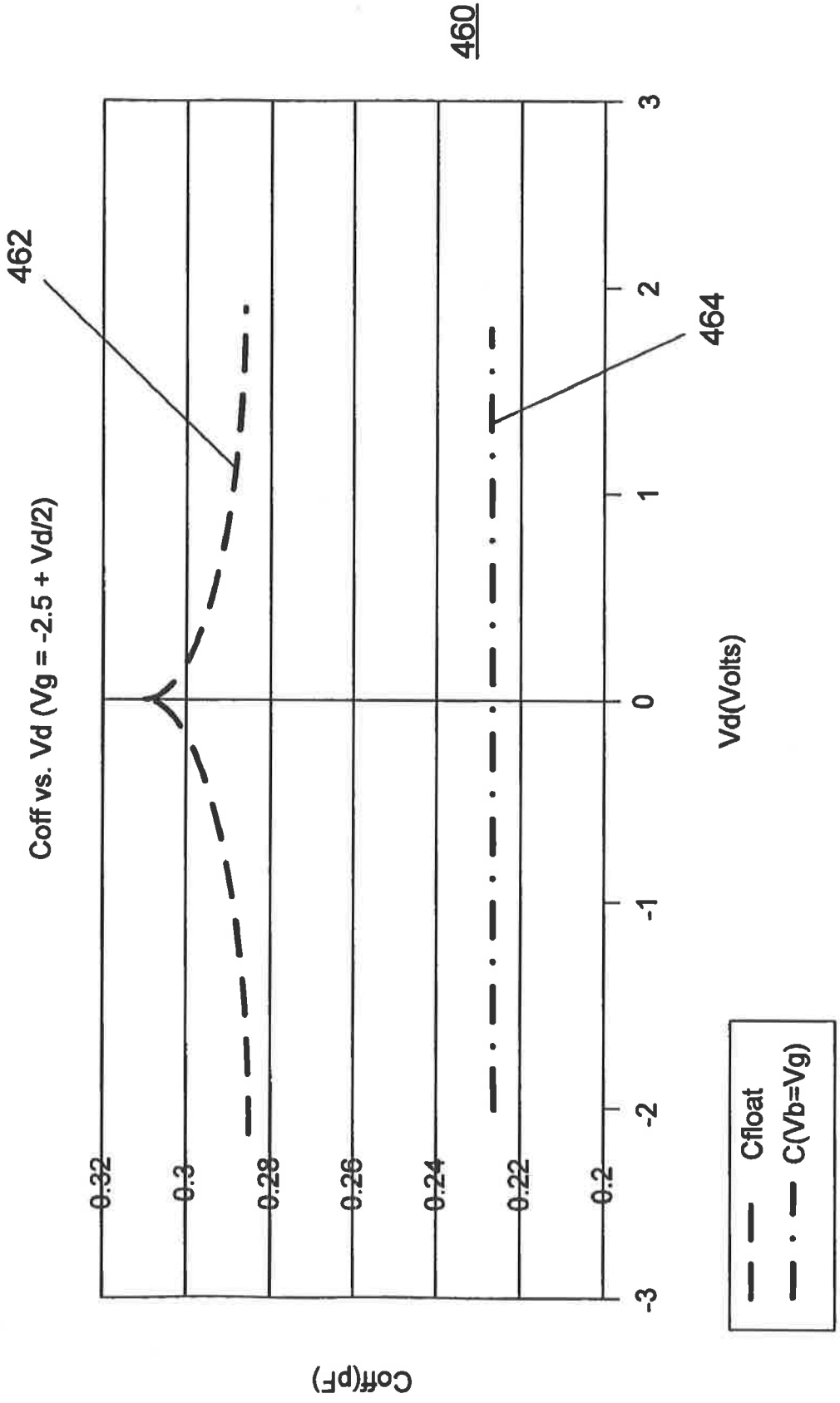

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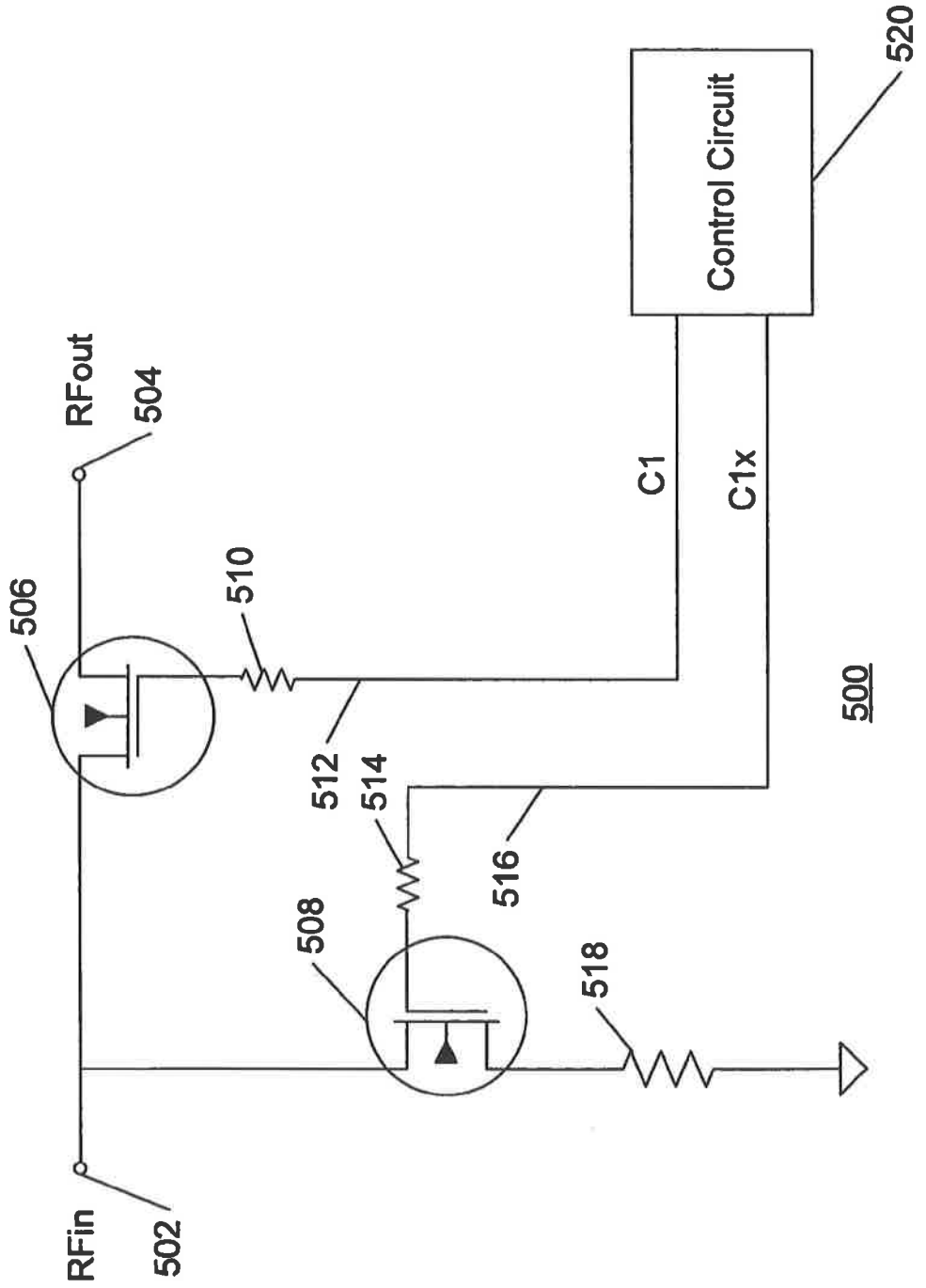

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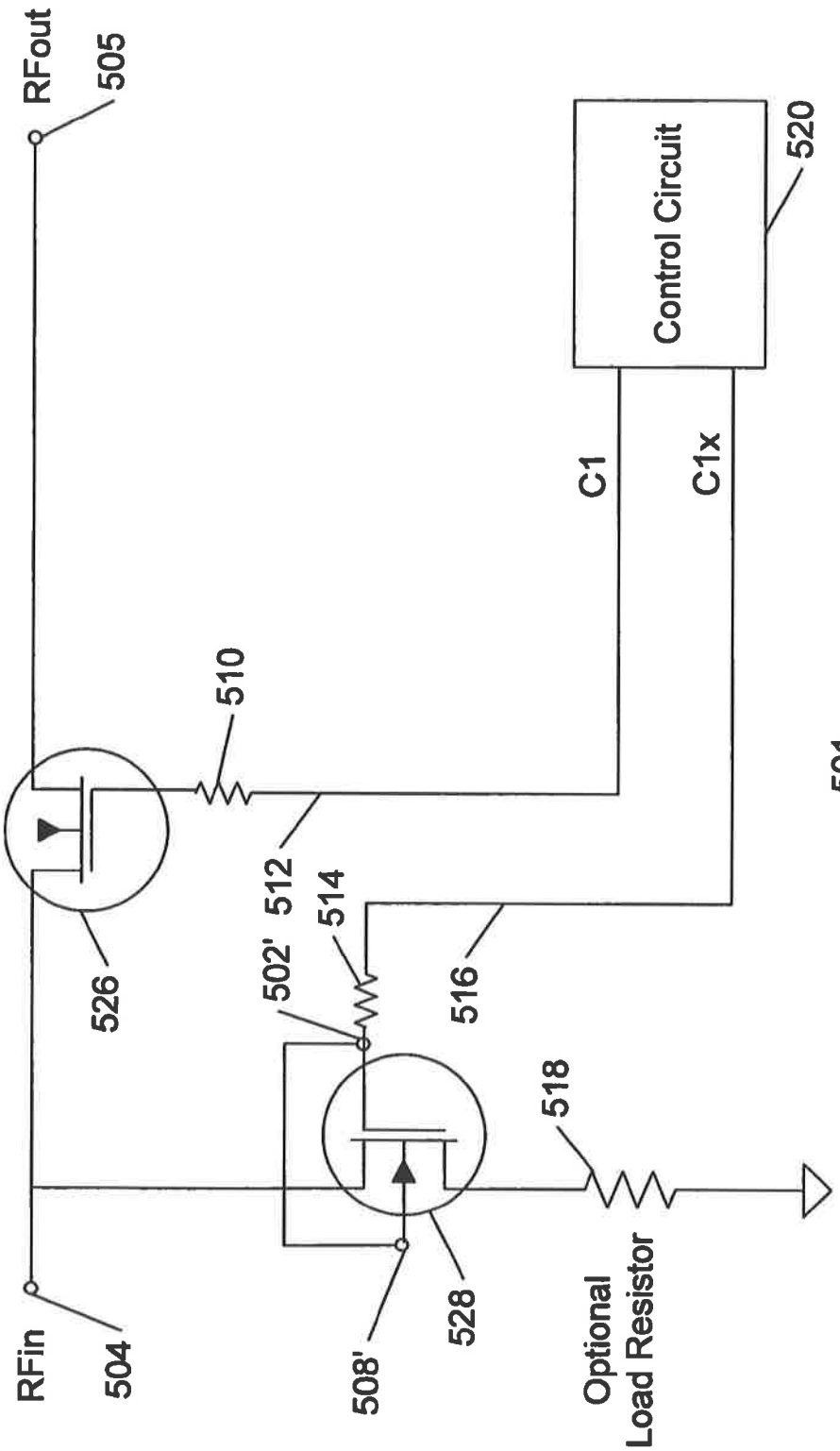
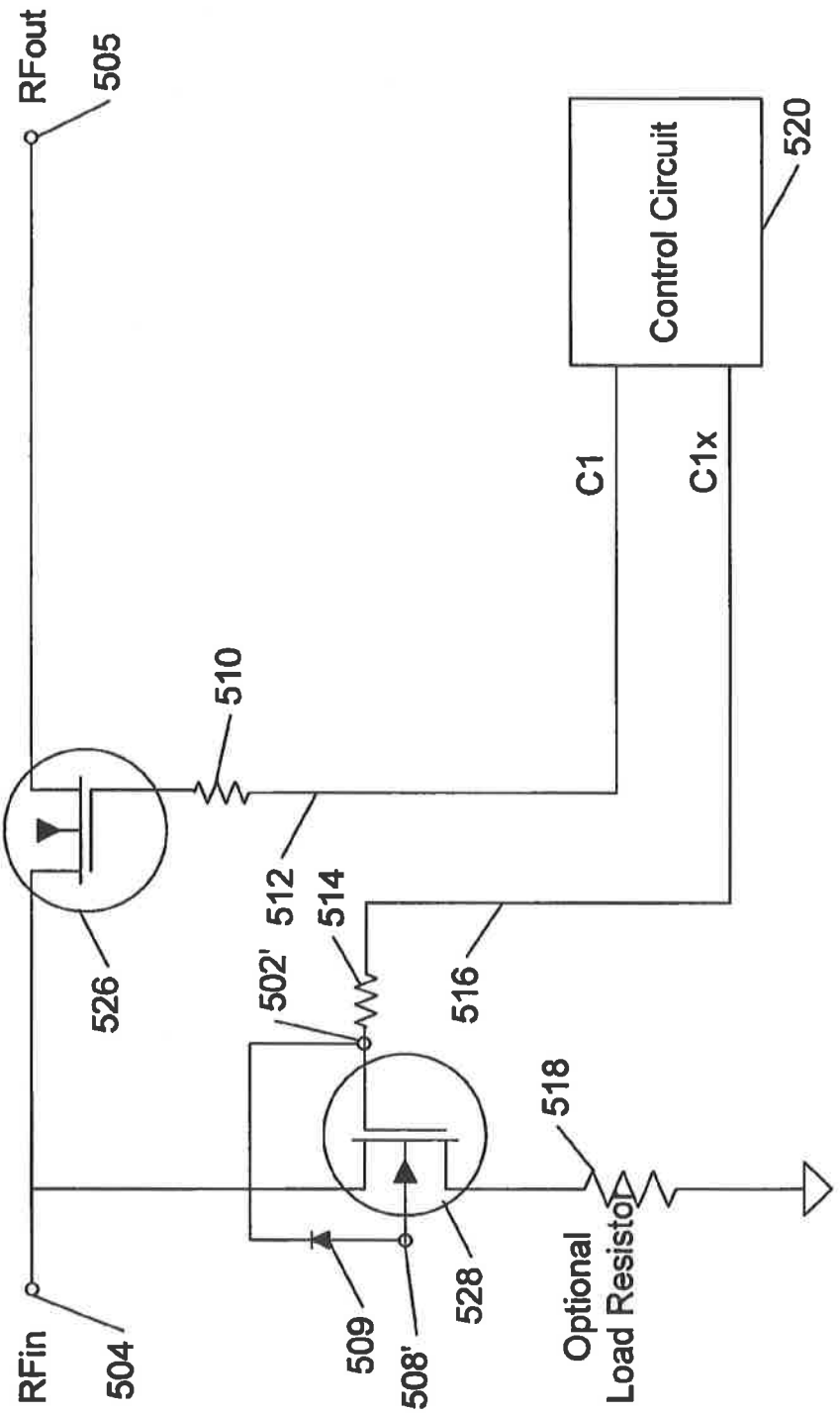


Figure 5B



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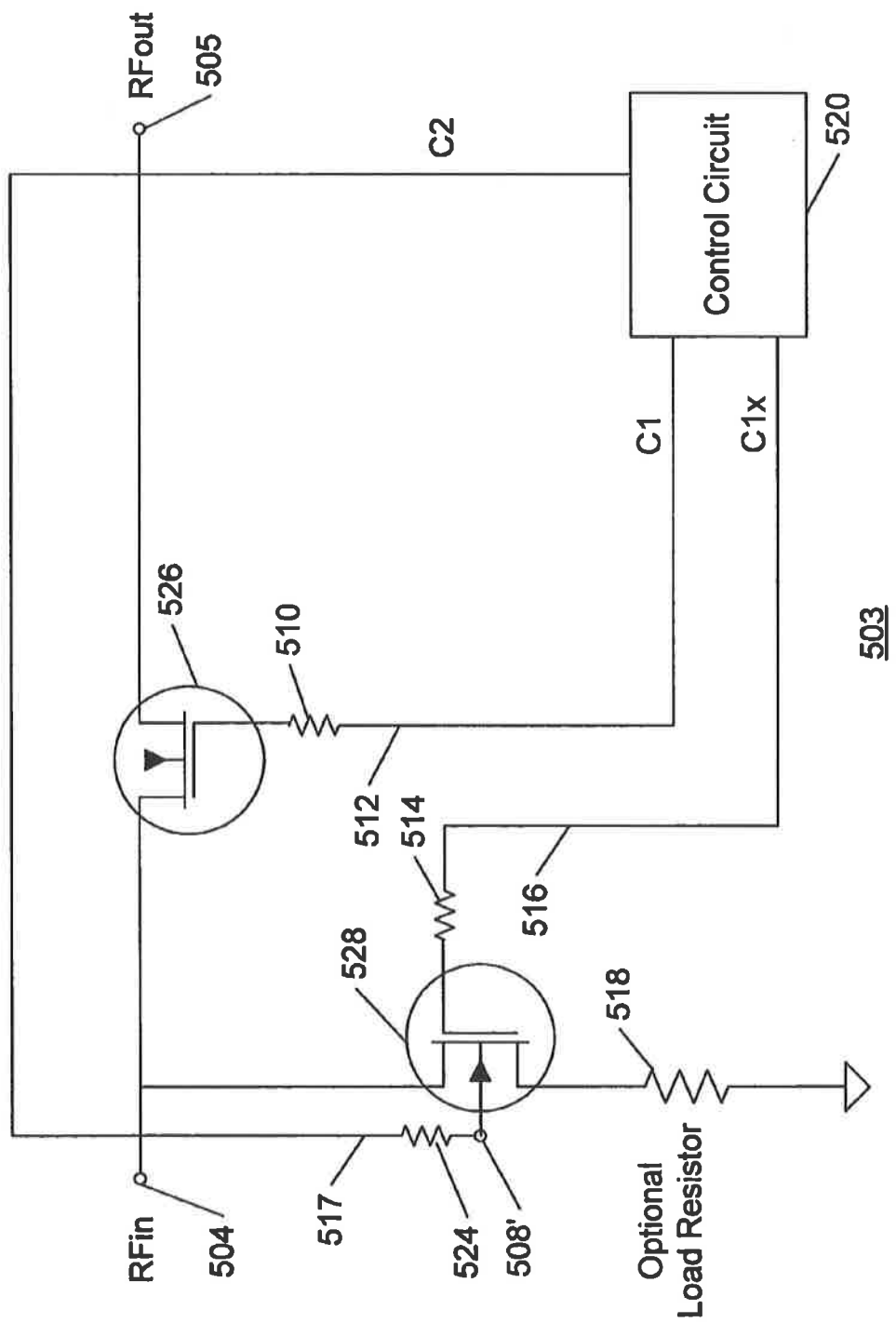

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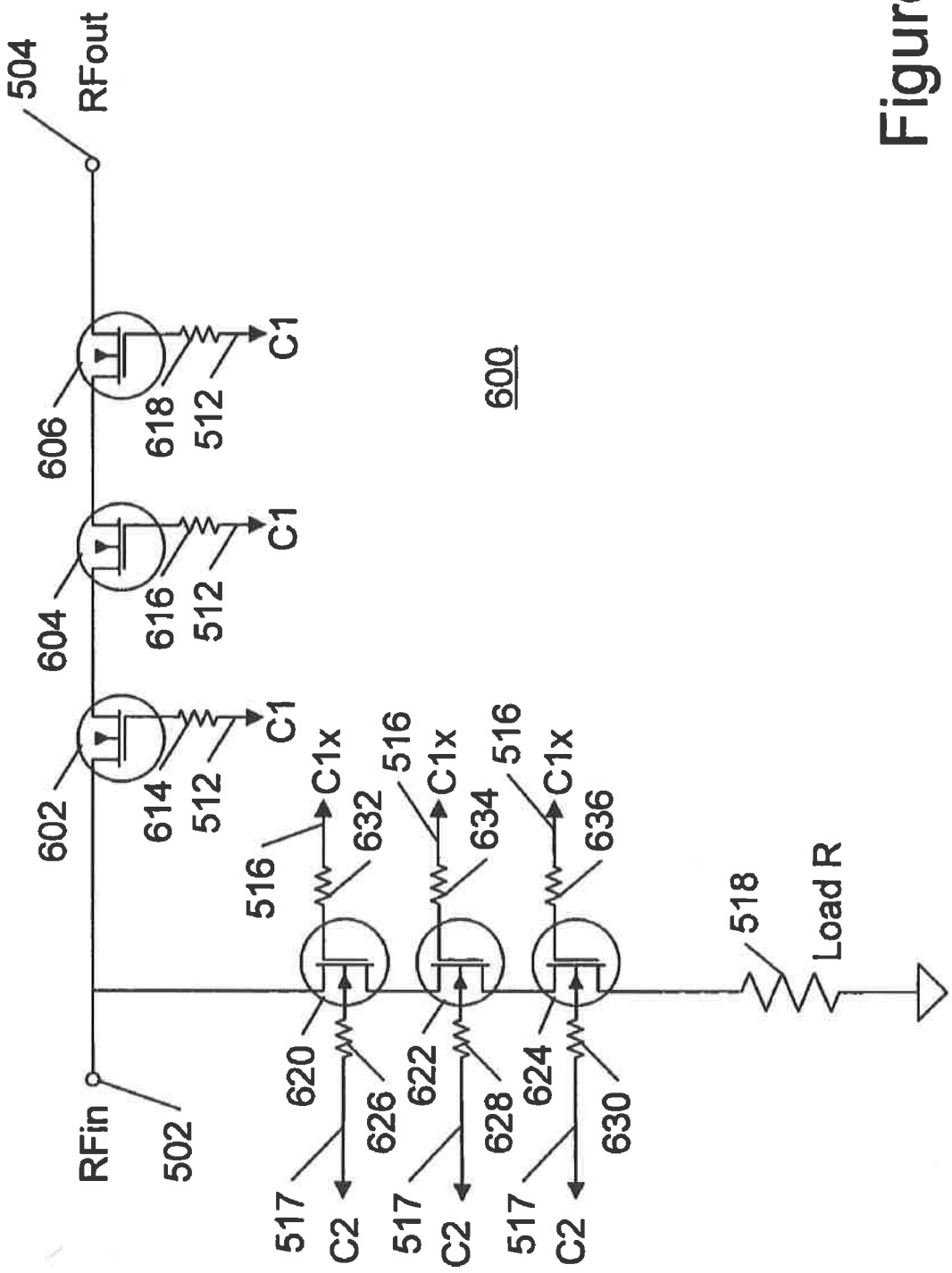

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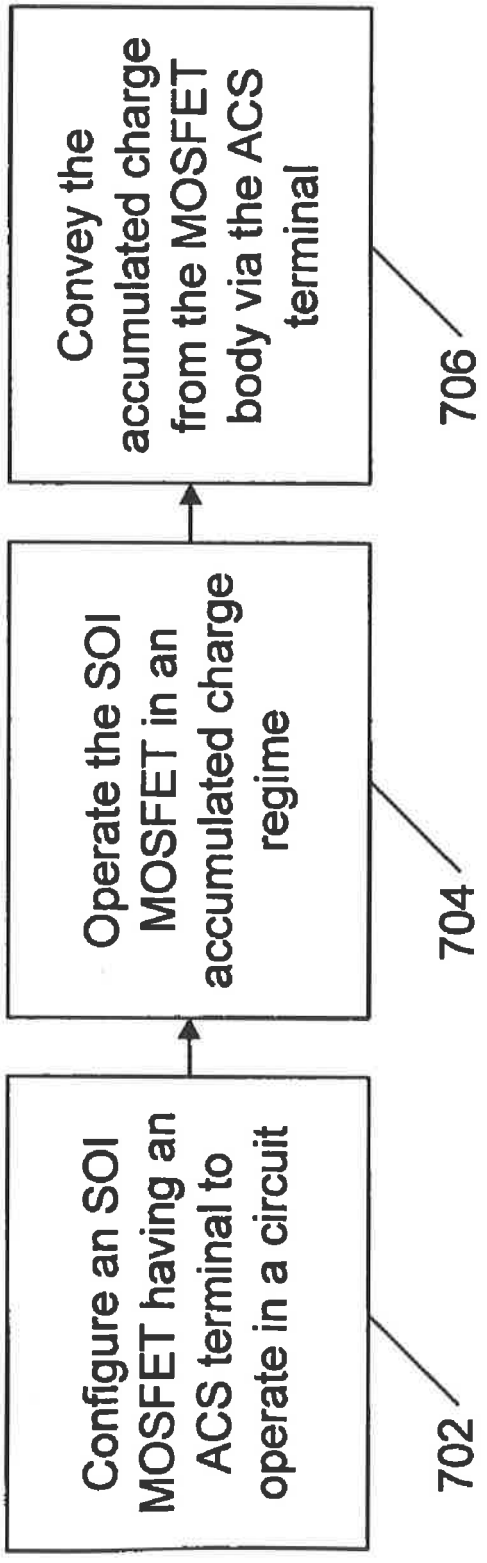

Figure 7

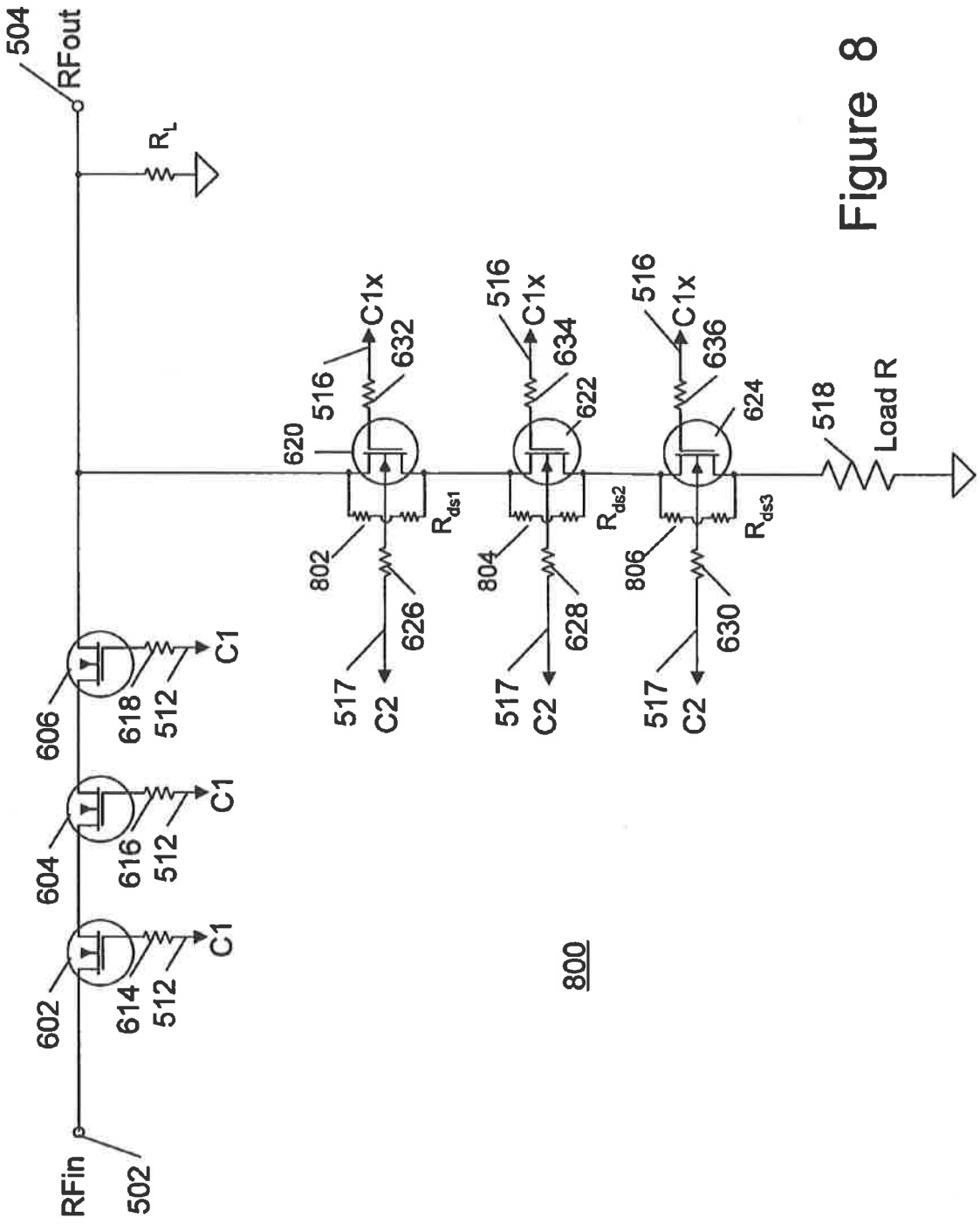

Figure 8

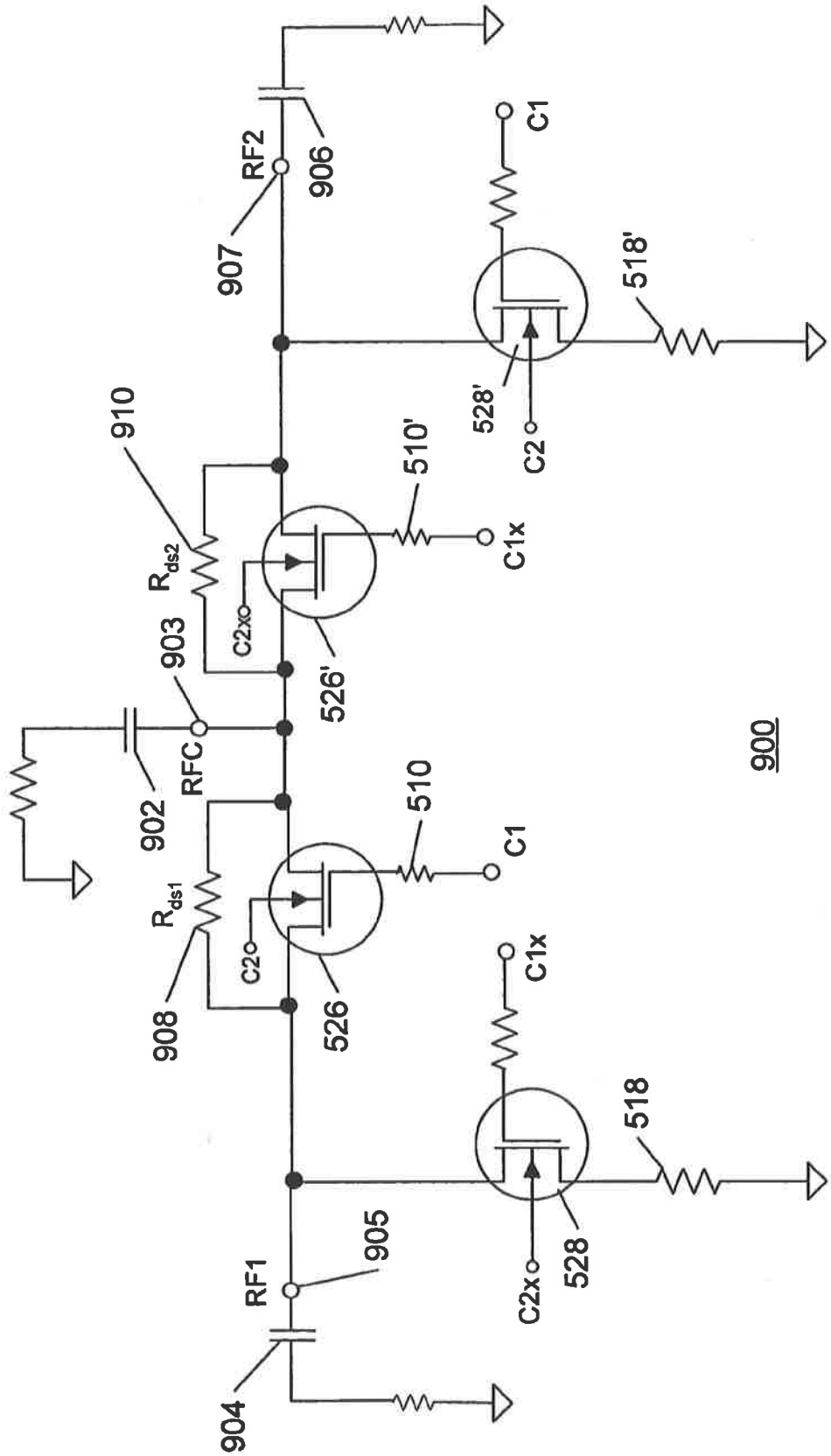

Figure 9

METHOD AND APPARATUS FOR USE IN IMPROVING LINEARITY OF MOSFET'S USING AN ACCUMULATED CHARGE SINK

CROSS-REFERENCE TO RELATED APPLICATIONS—CLAIM OF PRIORITY

This patent application claims the benefit of priority under 35 U.S.C. §119 (e) to commonly-assigned U.S. Provisional Application No. 60/698,523, filed Jul. 11, 2005, entitled "Method and Apparatus for use in Improving Linearity of MOSFETs using an Accumulated Charge Sink". This patent application is related to co-pending and commonly assigned U.S. Provisional Application No. 60/718,260, filed Sep. 15th, 2005, entitled "Method and Apparatus Improving Gate Oxide Reliability by Controlling Accumulated Charge", hereafter "the related application". The above-cited provisional patent applications, including both of their appendices, are hereby incorporated by reference herein in their entirety as if set forth in full.

BACKGROUND

1. Field

The present invention relates to metal-oxide-semiconductor (MOS) field effect transistors (FETs), and particularly to MOSFETs fabricated on Semiconductor-On-Insulator ("SOI") and Semiconductor-On-Sapphire ("SOS") substrates. In one embodiment, an SOI (or SOS) MOSFET is adapted to control accumulated charge and thereby improve linearity of circuit elements.

2. Description of Related Art

Although the disclosed method and apparatus for use in improving the linearity of MOSFETs are described herein as applicable for use in SOI MOSFETs, it will be appreciated by those skilled in the electronic device design arts that the present teachings are equally applicable for use in SOS MOSFETs. In general, the present teachings can be used in the implementation of MOSFETs using any convenient semiconductor-on-insulator technology, including silicon-on-insulator technology. For example, the inventive MOSFETs described herein can be implemented using compound semiconductors on insulating substrates. Such compound semiconductors include, but re not limited to, the following: Silicon Germanium (SiGe), Gallium Arsenide (GaAs), Indium Phosphide (InP), Gallium Nitride (GaN), Silicon Carbide (SiC), and II-VI compound semiconductors, including Zinc Selenide (ZnSe) and Zinc Sulfide (ZnS). The present teachings also may be used in implementing MOSFETs fabricated from thin-film polymers. Organic thin-film transistors (OTFTs) utilize a polymer, conjugated polymers, oligomers, or other molecules to form the insulting gate dielectric layer. The present inventive methods and apparatus may be used in implementing such OTFTs.

It will be appreciated by those skilled in the electronic design arts that the present disclosed method and apparatus apply to virtually any insulating gate technology, and to integrated circuits having a floating body. As those skilled in the art will appreciate, technologies are constantly being developed for achieving "floating body" implementations. For example, the inventors are aware of circuits implemented in bulk silicon wherein circuit implementations are used to "float" the body of the device. In addition, the disclosed method and apparatus can also be implemented using silicon-on-bonded wafer implementations. One such silicon-on-bonded wafer technique uses "direct silicon bonded" (DSB) substrates. Direct silicon bond (DSB) substrates are fabricated by bonding and electrically attaching a film of single-crystal silicon of differing crystal orientation onto a base substrate. The present disclosure therefore contemplates embodiments of the disclosed method and apparatus implemented in any of the developing floating body implementations. Therefore, references to and exemplary descriptions of SOI MOSFETs herein are not to be construed as limiting the applicability of the present teachings to SOI MOSFETs only. Rather, as described below in more detail, the disclosed method and apparatus find utility in MOSFETs implemented in a plurality of device technologies, including SOS and silicon-on-bonded wafer technologies.

As is well known, a MOSFET employs a gate-modulated conductive channel of n-type or p-type conductivity, and is accordingly referred to as an "NMOSFET" or "PMOSFET", respectively. FIG. **1** shows a cross-sectional view of an exemplary prior art SOI NMOSFET **100**. As shown in FIG. **1**, the prior art SOI NMOSFET **100** includes an insulating substrate **118** that may comprise a buried oxide layer, sapphire, or other insulating material. A source **112** and drain **116** of the NMOSFET **100** comprise N+ regions (i.e., regions that are heavily doped with an "n-type" dopant material) produced by ion implantation into a silicon layer positioned above the insulating substrate **118**. (The source and drain of PMOSFETs comprise P+ regions (i.e., regions heavily doped with "p-type" dopant material)). The body **114** comprises a P-region (i.e., a region that is lightly doped with a "p-type" dopant), produced by ion implantation, or by dopants already present in the silicon layer when it is formed on the insulating substrate **118**. As shown in FIG. **1**, the NMOSFET **100** also includes a gate oxide **110** positioned over the body **114**. The gate oxide **110** typically comprises a thin layer of an insulating dielectric material such as SiO_2. The gate oxide **110** electrically insulates the body **114** from a gate **108** positioned over the gate oxide **110**. The gate **108** comprises a layer of metal or, more typically, polysilicon.

A source terminal **102** is operatively coupled to the source **112** so that a source bias voltage "Vs" may be applied to the source **112**. A drain terminal **106** is operatively coupled to the drain **116** so that a drain bias voltage "Vd" may be applied to the drain **116**. A gate terminal **104** is operatively coupled to the gate **108** so that a gate bias voltage "Vg" may be applied to the gate **108**.

As is well known, when a voltage is applied between the gate and source terminals of a MOSFET, a generated electric field penetrates through the gate oxide to the transistor body. For an enhancement mode device, a positive gate bias creates a channel in the channel region of the MOSFET body through which current passes between the source and drain. For a depletion mode device, a channel is present for a zero gate bias. Varying the voltage applied to the gate modulates the conductivity of the channel and thereby controls the current flow between the source and drain.

For an enhancement mode MOSFET, for example, the gate bias creates a so-called "inversion channel" in a channel region of the body **114** under the gate oxide **110**. The inversion channel comprises carriers having the same polarity (e.g., "P" polarity (i.e., hole carriers), or "N" polarity (i.e., electron carriers) carriers) as the polarity of the source and drain carriers, and it thereby provides a conduit (i.e., channel) through which current passes between the source and the drain. For example, as shown in the SOI NMOSFET **100** of FIG. **1**, when a sufficiently positive voltage is applied between the gate **108** and the source **112** (i.e. a positive gate bias exceeding a threshold voltage V_{th}), an inversion channel is formed in the channel region of the body **114**. As noted above, the polarity of carriers in the inversion channel is

identical to the polarity of carriers in the source and drain. In this example, because the source and drain comprise "n-type" dopant material and therefore have N polarity carriers, the carriers in the channel comprise N polarity carriers. Similarly, because the source and drain comprise "p-type" dopant material in PMOSFETs, the carriers in the channel of turned on (i.e., conducting) PMOSFETs comprise P polarity carriers.

Depletion mode MOSFETs operate similarly to enhancement mode MOSFETs, however, depletion mode MOSFETs are doped so that a conducting channel exists even without a voltage being applied to the gate. When a voltage of appropriate polarity is applied to the gate the channel is depleted. This, in turn, reduces the current flow through the depletion mode device. In essence, the depletion mode device is analogous to a "normally closed" switch, while the enhancement mode device is analogous to a "normally open" switch. Both enhancement and depletion mode MOSFETs have a gate voltage threshold, V_{th}, at which the MOSFET changes from an off-state (non-conducting) to an on-state (conducting).

No matter what mode of operation an SOI MOSFET employs (i.e., whether enhancement or depletion mode), when the MOSFET is operated in an off-state (i.e., the gate voltage does not exceed V_{th}), and when a sufficient nonzero gate bias voltage is applied with respect to the source and drain, an "accumulated charge" may occur under the gate. The "accumulated charge", as defined in more detail below and used throughout the present application, is similar to the "accumulation charge" described in the prior art literature in reference to MOS capacitors. However, the prior art references describe "accumulation charge" as referring only to bias-induced charge existing under a MOS capacitor oxide, wherein the accumulation charge is of the same polarity as the majority carriers of the semiconductor material under the capacitor oxide. In contrast, and as described below in more detail, "accumulated charge" is used herein to refer to gate-bias induced carriers that may accumulate in the body of an off-state MOSFET, even if the majority carriers in the body do not have the same polarity as the accumulated charge. This situation may occur, for example, in an off-state depletion mode NMOSFET, wherein the accumulated charge may comprise holes (i.e., having P polarity) even though the body doping is N– rather than P–.

For example, as shown in FIG. **1**, when the SOI NMOSFET **100** is biased to operate in an off-state, and when a sufficient nonzero voltage is applied to the gate **108**, an accumulated charge **120** may accumulate in the body **114** underneath and proximate the gate oxide **110**. The operating state of the SOI NMOSFET **100** shown in FIG. **1** is referred to herein as an "accumulated charge regime" of the MOSFET. The accumulated charge regime is defined in more detail below. The causes and effects of the accumulated charge in SOI MOSFETs are now described in more detail.

As is well known, electron-hole pair carriers may be generated in MOSFET bodies as a result of several mechanisms (e.g., thermal, optical, and band-to-band tunneling electron-hole pair generation processes). When electron-hole pair carriers are generated within an NMOSFET body, for example, and when the NMOSFET is biased in an off-state condition, electrons may be separated from their hole counterparts and pulled into both the source and drain. Over a period of time, assuming the NMOSFET continues to be biased in the off-state, the holes (resulting from the separated electron-hole pairs) may accumulate under the gate oxide (i.e., forming an "accumulated charge") underneath and proximate the gate oxide. A similar process (with the behavior of electrons and holes reversed) occurs in similarly biased PMOSFET devices. This phenomenon is now described with reference to the SOI NMOSFET **100** of FIG. **1**.

When the SOI NMOSFET **100** is operated with gate, source and drain bias voltages that deplete the channel carriers in the body **114** (i.e., the NMOSFET **100** is in the off-state), holes may accumulate underneath and proximate the gate oxide **110**. For example, if the source bias voltage Vs and the drain bias voltage Vd are both zero (e.g., connected to a ground contact, not shown), and the gate bias voltage Vg comprises a sufficiently negative voltage with respect to ground and with respect to V_{th}, holes present in the body **114** become attracted to the channel region proximate the gate oxide **110**. Over a period of time, unless removed or otherwise controlled, the holes accumulate underneath the gate oxide **110** and result in the accumulated charge **120** shown in FIG. **1**. The accumulated charge **120** is therefore shown as positive "+" hole carriers in FIG. **1**. In the example given, Vg is negative with respect to Vs and Vd, so electric field regions **122** and **124** may also be present.

Accumulated Charge Regime Defined

The accumulated charge is opposite in polarity to the polarity of carriers in the channel. Because, as described above, the polarity of carriers in the channel is identical to the polarity of carriers in the source and drain, the polarity of the accumulated charge **120** is also opposite to the polarity of carriers in the source and drain. For example, under the operating conditions described above, holes (having "P" polarity) accumulate in off-state NMOSFETs, and electrons (having "N" polarity) accumulate in off-state PMOSFETs. Therefore, a MOSFET device is defined herein as operating within the "accumulated charge regime" when the MOSFET is biased to operate in an off-state, and when carriers having opposite polarity to the channel carriers are present in the channel region. Stated in other terms, a MOSFET is defined as operating within the accumulated charge regime when the MOSFET is biased to operate in an off-state, and when carriers are present in the channel region having a polarity that is opposite the polarity of the source and drain carriers.

For example, and referring again to FIG. **1**, the accumulated charge **120** comprises hole carriers having P or "+" polarity. In contrast, the carriers in the source, drain, and channel (i.e., when the FET is in the on-state) comprise electron carriers having N or "–" polarity. The SOI NMOSFET **100** is therefore shown in FIG. **1** as operating in the accumulated charge regime. It is biased to operate in an off-state, and an accumulated charge **120** is present in the channel region. The accumulated charge **120** is opposite in polarity (P) to the polarity of the channel, source and drain carriers (N).

In another example, wherein the SOI NMOSFET **100** comprises a depletion mode device, V_{th} is negative by definition. According to this example, the body **114** comprises an N– region (as contrasted with the P– region shown in FIG. **1**). The source and drain comprise N+ regions similar to those shown in the enhancement mode MOSFET **100** of FIG. **1**. For Vs and Vd both at zero volts, when a gate bias Vg is applied that is sufficiently negative relative to V_{th} (for example, a Vg that is more negative than approximately –1 V relative to V_{th}), the depletion mode NMOSFET is biased into an off-state. If biased in the off-state for a sufficiently long period of time, holes may accumulate under the gate oxide and thereby comprise the accumulated charge **120** shown in FIG. **1**.

In other examples, Vs and Vd may comprise nonzero bias voltages. In some embodiments, Vg must be sufficiently negative to both Vs and Vd (in order for Vg to be sufficiently negative to V_{th}, for example) in order to bias the NMOSFET in the off-state. Those skilled in the MOSFET device design arts shall recognize that a wide variety of bias voltages may be

used to practice the present teachings. As described below in more detail, the present disclosed method and apparatus contemplates use in any SOI MOSFET device biased to operate in the accumulated charge regime.

SOI and SOS MOSFETs are often used in applications in which operation within the accumulated charge regime adversely affects MOSFET performance. As described below in more detail, unless the accumulated charge is removed or otherwise controlled, it detrimentally affects performance of SOI MOSFETs under certain operating conditions. One exemplary application, described below in more detail with reference to the circuits shown in FIGS. **2**B and **5**A, is the use of SOI MOSFETs in the implementation of radio frequency (RF) switching circuits. As described below with reference to FIGS. **2**B and **5**A in more detail, the inventors have discovered that unless the accumulated charge is removed or otherwise controlled, under some operating conditions, the accumulated charge adversely affects the linearity of the SOI MOSFET and thereby increases harmonic distortion and intermodulation distortion (IMD) caused by the MOSFET when used in the implementation of certain circuits. In addition, as described below in more detail, the inventors have discovered that removal or control of the accumulated charge improves the drain-to-source breakdown voltage (i.e., the "BVDSS") characteristics of the SOI MOSFETs.

Therefore, it is desirable to provide techniques for adapting and improving SOI (and SOS) MOSFETs, and circuits implemented with the improved SOI MOSFETs, in order to remove or otherwise control the accumulated charge, and thereby significantly improve SOI MOSFET performance. It is desirable to provide methods and apparatus for use in improving the linearity characteristics in SOI MOSFETs. The improved MOSFETs should have improved linearity, harmonic distortion, intermodulation distortion, and BVDSS characteristics as compared with prior art MOSFETs, and thereby improve the performance of circuits implemented with the improved MOSFETs. The present teachings provide such novel methods and apparatus.

SUMMARY

Apparatuses and methods are provided to control accumulated charge in SOI MOSFETs, thereby improving nonlinear responses and harmonic and intermodulaton distortion effects in the operation of the SOI MOSFETs.

In one embodiment, a circuit having at least one SOI MOSFET is configured to operate in an accumulated charge regime. An accumulated charge sink (ACS), operatively coupled to the body of the SOI MOSFET, receives accumulated charge generated in the body, thereby reducing the nonlinearity of the net source-drain capacitance of the SOI MOSFET.

In one embodiment, the ACS comprises a high impedance connection to the MOSFET body, with an exemplary impedance greater than 10^6 ohm.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view of an exemplary prior art SOI NMOSFET.

FIG. **2**A is a simplified schematic of an electrical model showing the off-state impedance characteristics of the exemplary prior art SOI NMOSFET of of FIG. **1**.

FIG. **2**B is a schematic of an exemplary simplified RF switching circuit implemented using prior art SOI MOSFETs such as the prior art SOI NMOSFET of FIG. **1**.

FIGS. **3**A and **3**B are simplified schematic diagrams of a top view of an improved SOI NMOSFET adapted to control accumulated charge in accordance with the present teachings.

FIG. **3**C is a cross-sectional perspective schematic of an improved SOI NMOSFET adapted to control accumulated charge showing gate, source, drain and accumulated charge sink (ACS) terminals.

FIG. **3**D is a simplified top view schematic of an improved SOI NMOSFEET adapted to control accumulated charge having an accumulated charge sink (ACS) electrically coupled to a P+ region.

FIG. **3**E is a simplified top view schematic of an improved SOI NMOSFET adapted to control accumulated charge and showing a cross-sectional view line A-A' taken along approximately a center of the SOI NMOSFET.

FIG. **3**F is a cross-sectional view of the improved SOI NMOSET of FIG. **3**E taken along the A-A' view line of FIG. **3**E.

FIG. **3**G is a cross-sectional view of the improved SOI NMOSET of FIGS. **3**A-**3**B.

FIG. **3**H is a simplified top view schematic of an SOI NMOSFET illustrating a region of increased threshold voltage that can occur in prior art MOSFETs and in some embodiments of the improved SOI MOSFET due to manufacturing processes.

FIG. **3**I is a plot of inversion channel charge as a function of applied gate voltage when a region of increased threshold voltage is present in an SOI MOSFET.

FIG. **3**J is a simplified top view schematic of an improved SOI NMOSFET adapted to control accumulated charge and configured in a "T-gate" configuration.

FIG. **3**K is a simplified top view schematic of an improved SOI NMOSFET adapted to control accumulated charge and configured in an "H-gate" configuration.

FIG. **4**A is a simplified schematic of an improved SOI NMOSFET adapted to control accumulated charge embodied as a four terminal device.

FIG. **4**B is a simplified schematic of an improved SOI NMOSFET adapted to control accumulated charge, embodied as a four terminal device, wherein an accumulated charge sink (ACS) terminal is coupled to a gate terminal.

FIG. **4**C is a simplified schematic of an improved SOI NMOSFET adapted to control accumulated charge, embodied as a four terminal device, wherein an accumulated charge sink (ACS) terminal is coupled to a gate terminal via a diode.

FIG. **4**D is a simplified schematic of an improved SOI NMOSFET adapted to control accumulated charge, embodied as a four terminal device, wherein an accumulated charge sink (ACS) terminal is coupled to a control circuit.

FIG. **4**E is a simplified schematic of an exemplary RF switch circuit implemented using the four terminal ACC NMOSFET of FIG. **4**D, wherein the ACS terminal is driven by an external bias source.

FIG. **4**F is a simplified schematic of an improved SOI NMOSFET adapted to control accumulated charge, embodied as a four terminal device, wherein an accumulated charge sink (ACS) terminal is coupled to a clamping circuit.

FIG. **4**G is a simplified schematic of an improved SOI NMOSFET adapted to control accumulated charge, embodied as a four terminal device, wherein an accumulated charge sink (ACS) terminal is coupled to a gate terminal via a diode in parallel with a capacitor.

FIG. **4**H shows plots of the off-state capacitance (C_{off}) versus applied drain-to-source voltages for SOI MOSFETs operated in the accumulated charge regime, wherein a first plot shows the off-state capacitance C_{off} of a prior art SOI MOSFET, and wherein a second plot shows the off-state

capacitance C_{off} of the improved ACC SOI MOSFET made in accordance with the present teachings.

FIG. **5**A is a schematic of an exemplary prior art single pole, single throw (SPST) radio frequency (RF) switch circuit.

FIG. **5**B is a schematic of an RF switch circuit adapted for improved performance using accumulated charge control, wherein the gate of a shunting SOI NMOSFET is coupled to an accumulated charge sink (ACS) terminal.

FIG. **5**C is a schematic of an RF switch circuit adapted for improved performance using accumulated charge control, wherein the gate of a shunting SOI NMOSFET is coupled to an accumulated charge sink (ACS) terminal via a diode.

FIG. **5**D is a schematic of an RF switch circuit adapted for improved performance using accumulated charge control, wherein the accumulated charge sink (ACS) terminal is coupled to a control circuit.

FIG. **6** is a schematic of an RF switch circuit including stacked MOSFETs, adapted for improved performance using accumulated charge control, wherein the accumulated charge sink (ACS) terminals of the shunting stacked MOSFETs are coupled to a control signal.

FIG. **7** shows a flowchart of an exemplary method of improving the linearity of an SOI MOSFET device using an accumulated charge sink in accordance with the present disclosure.

FIG. **8** shows a simplified circuit schematic of an exemplary embodiment of an RF switch circuit made in accordance with the present disclosure, wherein the RF switch circuit includes drain-to-source resistors between the drain and source of the ACC MOSFETs.

FIG. **9** shows a simplified schematic of an exemplary single-pole double-throw (SPDT) RF switch circuit made in accordance with the present disclosure, wherein drain-to-source resistors are shown across the switching ACC SOI MOSFETs.

Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION

As noted above, those skilled in the electronic device design arts shall appreciate that the teachings herein apply equally to NMOSFETs and PMOSFETs. For simplicity, the embodiments and examples presented herein for illustrative purposes include only NMOSFETs, unless otherwise noted. By making well known changes to dopants, charge carriers, polarity of bias voltages, etc., persons skilled in the arts of electronic devices will easily understand how these embodiments and examples may be adapted for use with PMOSFETs.

Non-Linearity and Harmonic Distortion Effects of Accumulated Charge in an SOI NMOSFET

As described above in the background, no matter what mode of operation the MOSFET employs (i.e., enhancement mode or depletion mode), under some circumstances, when a MOSFET is operated in an off-state with a nonzero gate bias voltage applied with respect to the source and drain, an accumulated charge may occur under the gate. According to the present teachings, as described above when the MOSFET is in an off-state, and when carriers are present in the channel region having a polarity that is opposite the polarity of the source and drain carriers, the MOSFET is defined herein as operating in the accumulated charge regime.

According to the present teachings, the inventors have observed that, when used in certain circuit implementations, MOSFETs operating in the accumulated charge regime exhibit undesirable non-linear characteristics that adversely impact circuit performance. For example, as described below in more detail with reference to FIG. **2**A, the accumulated charge **120** (FIG. **1**) adversely affects the linearity of off-state SOI MOSFETs, and more specifically, it adversely affects the linearity of contributing capacitances to the drain-to-source capacitance (Cds). For an SOI MOSFET operating in an off-state, Cds is referred to as C_{off}. The contributing capacitances to C_{off} are described below in reference to FIG. **2**A for bias conditions wherein the gate bias Vg is provided by a circuit having an impedance that is large compared to the impedances of the contributing capacitances. As described below with reference to FIGS. **2**B and **5**A, this, in turn, adversely affects harmonic distortion, intermodulation distortion, and other performance characteristics of circuits implemented with the SOI MOSFETs. These novel observations, not taught or suggested by the prior art, may be understood with reference to the electrical model shown in FIG. **2**A.

FIG. **2**A is a simplified schematic of an electrical model **200** showing the off-state impedance (or conversely, conductance) characteristics of the exemplary prior art SOI NMOSFET **100** of FIG. **1**. More specifically, the model **200** shows the impedance characteristics from the source **112** to the drain **116** when the NMOSFET **100** is operated in the off-state. Because the drain-to-source off-state impedance characteristic of the NMOSFET **100** is primarily capacitive in nature, it is referred to herein as the drain-to-source off-state capacitance (C_{off}). For the exemplary description herein, the gate **108** is understood to be biased at a voltage Vg by a circuit (not shown) that has an impedance that is large compared to the impedances of the contributing capacitances described in reference to FIG. **2**A. Persons skilled in the electronic arts will understand how this exemplary description may be modified for the case wherein the impedance of the circuit providing the Vg bias is not large compared to the impedances of the contributing capacitances.

As shown in FIG. **2**A, the junction between the source **112** and the body **114** (i.e., a source-body junction **218**) of the off-state NMOSFET **100** can be represented by a junction diode **208** and a junction capacitor **214**, configured as shown. Similarly, the junction between the drain **116** and the body **114** (i.e., the drain-body junction **220**) of the off-state NMOSFET **100** can be represented by a junction diode **210** and a junction capacitor **216**, configured as shown. The body **114** is represented simply as an impedance **212** that is present between the source-body junction **218** and the drain-body junction **220**.

A capacitor **206** represents the capacitance between the gate **108** and the body **114**. A capacitor **202** represents the capacitance between the source **112** and the gate **108**, and another capacitor **204** represents the capacitance between the drain **116** and the gate **108**. A substrate capacitance due to the electrical coupling between the source **112** and the drain **116** (through the insulating substrate **118** shown in FIG. **1**) is taken to be negligibly small in the exemplary description set forth below, and therefore is not shown in the electrical model **200** of FIG. **2**A.

As described above, when the NMOSFET **100** is in the off-state, and when the accumulated charge **120** (FIG. **1**) is not present in the body **114** (i.e., the NMOSFET **100** is not operating within the accumulated charge regime), the body **114** is depleted of charge carriers. In this case the body impedance **212** is analogous to the impedance of an insulator, and the electrical conductance through the body **114** is very small (i.e., the NMOSFET **100** is in the off-state). Consequently, the principal contributions to the drain-to-source off-state

capacitance C_{off} are provided by the capacitors **202** and **204**. The capacitors **202** and **204** are only slightly voltage dependent, and therefore do not significantly contribute to a nonlinear response that adversely affects harmonic generation and intermodulation distortion characteristics.

However, when the NMOSFET **100** operates within the accumulated charge regime, and the accumulated charge **120** is therefore present in the body **114**, mobile holes comprising the accumulated charge produce p-type conductivity between the source-body junction **218** and the drain-body junction **220**. In effect, the accumulated charge **120** produces an impedance between the source-body junction **218** and the drain-body junction **220** that is significantly less than the impedance between the junctions in the absence of the accumulated charge. If a Vds voltage is applied between the drain **116** and the source **112**, the mobile holes redistribute according to the electrical potentials that result within the body **114**. DC and low-frequency current flow through the SOI NMOSFET **100** is prevented by the diode properties of the source-body junction **218** and the drain-body junction **220**, as represented by the junction diodes **208** and **210**, respectively. That is, because the junction diodes **208** and **210** are anti-series (i.e., "back-to-back") in this case, no DC or low-frequency currents flow through the SOI NMOSFET **100**. However, high-frequency currents may flow through the SOI NMOSFET **100** via the capacitances of the source-body junction **218** and the drain-body junction **220**, as represented by the junction capacitors **214** and **216**, respectively.

The junction capacitors **214** and **216** are voltage dependent because they are associated with junctions between n-type and p-type regions. This voltage dependence results from the voltage dependence of the width of the depletion region of the junction between the n-type and p-type regions. As a bias voltage is applied to the NMOSFET, the width of the depletion region of the junction between the n-type and p-type regions is varied. Because the capacitance of the junction depends on the width of the junction depletion region, the capacitance also varies as a function of the bias applied across the junction (i.e., the capacitance is also voltage dependent).

Further, the capacitors **202** and **204** may also have a voltage dependence caused by the presence of the accumulated charge **120**. Although the complex reasons for this voltage dependence are not described in detail herein, persons skilled in the arts of electronic devices shall understand that electric field regions (e.g., electric field regions **122** and **124** described above with reference to FIG. **1**) may be affected by the response of the accumulated charge and its response to an applied Vds, thereby causing a voltage dependence of capacitors **202** and **204**. An additional nonlinear effect may occur due to a direct capacitance (not shown) between the source **112** and the drain **116**. Although this direct capacitance would usually be expected to be negligible for most SOI MOSFETs, it may contribute for SOI MOSFETs having very short spacing between the source and drain. The contribution of this direct capacitance to C_{off} is also voltage-dependent in the presence of an accumulated charge, for reasons that are analogous to the voltage dependencies of the capacitors **202** and **204** as described above.

The voltage dependencies of the junction capacitors **214** and **216**, the gate-to-source and gate-to-drain capacitors **202**, **204**, respectively, and the direct capacitance (not shown), cause nonlinear behavior in off-state capacitance C_{off} of the MOSFET when AC voltages are applied to the NMOSFET **100**, thereby producing undesirable generation of harmonic distortions and intermodulation distortion (IMD). The relative contributions of these effects are complex, and depend on fabrication processes, biases, signal amplitudes, and other variables. However, those skilled in the electronic device design arts shall understand from the teachings herein that reducing, removing, or otherwise controlling the accumulated charge provides an overall improvement in the nonlinear behavior of C_{off}. In addition, because the body impedance **212** is significantly decreased in the presence of the accumulated charge **120**, the magnitude of C_{off} may be increased when the FET operates in the accumulated charge regime. Reducing, removing, or otherwise controlling the accumulated charge also mitigates this effect.

In addition, the accumulated charge does not accumulate in the body in an instant as soon as the FET transitions from an on-state (conducting state) to an off-state (non-conducting state). Rather, when the FET transitions from the on-state to the off-state, it begins to accumulate charge in the body of the MOSFET, and the amount of accumulated charge increases over time. The accumulation of the accumulated charge therefore has an associated time constant (i.e., it does not instantly reach a steady-state level of accumulated charge). The accumulated charge accumulates slowly in the FET body. The depleted FET has a C_{off} associated with it which is increased with an increasing amount of accumulated charge. In terms of FET performance, as the C_{off} increases with an increasing amount of accumulated charge in the FET body, drift occurs in the FET insertion loss (i.e., the FET becomes more "lossy"), isolation (the FET becomes less isolating) and insertion phase (delay in the FET is increased). Reducing, removing, or otherwise controlling the accumulated charge also mitigates these undesirable drift effects.

The inventors have observed that the nonlinear behavior of the MOSFET off-state capacitance C_{off} adversely affects the performance of certain circuits implemented with the prior art SOI MOSFETs. For example, when an RF switch is implemented using the prior art SOI MOSFETs, such as the prior art SOI NMOSFET **100** of FIG. **1**, the above-described nonlinear off-state characteristics of the prior art MOSFETs adversely affect the linearity of the switch. As described below in more detail, RF switch linearity is an important design parameter in many applications. Improved switch linearity leads to improved suppression of harmonic and intermodulation (IM) distortion of signals processed by the switch. These improved switch characteristics can be critically important in some applications such as use in cellular communication devices.

For example, the well known GSM cellular communication system standard imposes stringent linearity, harmonic and intermodulation suppression, and power consumption requirements on front-end components used to implement GSM cell phones. One exemplary GSM standard requires that all harmonics of a fundamental signal be suppressed to below −30 dBm at frequencies up to 12.75 GHz. If harmonics are not suppressed below these levels, reliable cell phone operation can be significantly adversely impacted (e.g., increased dropped calls or other communication problems may result due to harmonic and intermodulation distortion of the transmit and receive signals). Because the RF switching function is generally implemented in the cell phone front-end components, improvements in the RF switch linearity, harmonic and intermodulation suppression, and power consumption performance characteristics is highly desirable. A description of how the non-linear behavior of the off-state capacitance C_{off} of the prior art MOSFETs adversely affects these RF switch characteristics is now described with reference to FIG. **2B**.

Harmonic Distortion Effects on RF Switch Circuits Implemented Using Prior Art SOI MOSFETs

FIG. **2**B illustrates an exemplary simplified RF switch circuit **250** implemented using prior art MOSFETs such as the prior art SOI NMOSFET **100** described above with reference to FIG. **1**. A detailed description of the operation and implementation of RF switch circuits is provided in commonly assigned U.S. Pat. No. 6,804,502 which is hereby incorporated herein by reference in its entirety for its teachings on RF switch circuits. As shown in FIG. **2**B, the prior art RF switch **250** includes a single "pass" or "switching" MOSFET **254** operatively coupled to five shunting MOSFETs **260***a*-**260***e*.

The MOSFET **254** acts as a pass or switching transistor and is configured, when enabled, to selectively couple an RF input signal (applied to its drain, for example) to an RF antenna **258** via a transmission path **256**. The shunting MOSFETs, **260***a*-**260***e*, when enabled, act to alternatively shunt the RF input signal to ground. As is well known, the switching MOSFET **254** is selectively controlled by a first switch control signal (not shown) coupled to its gate, and the shunting MOSFETs, **260***a*-**260***e* are similarly controlled by a second switch control signal (not shown) coupled to their gates. The switching MOSFET **254** is thereby enabled when the shunting MOSFETs **260***a*-**260***e* are disabled, and vice versa. As shown in the exemplary embodiment of the RF switch **250** of FIG. **2**B, the switching MOSFET **254** is enabled by applying a gate bias voltage of +2.5V (via the first switch control signal). The shunting MOSFETs **260***a*-**260***e* are disabled by applying a gate bias voltage of −2.5V (via the second switch control signal).

When the switch **250** is configured in this state, the RF signal **252** propagates through the switching MOSFET **254**, through the transmission path **256**, and to the antenna **258**. As described above with reference to FIG. **2**A, when the shunting MOSFETS **260***a*-**260***e* comprise prior art SOI (or SOS) MOSFETs, such as the SOI NMOSFET **100** (FIG. **1**), an accumulated charge can occur in the SOI MOSFET bodies (i.e., when the SOI MOSFETs operate in the accumulated charge regime as described above). The accumulated charge can produce nonlinear behavior in the off-state capacitance C_{off} of the SOI MOSFETs when AC voltages are applied to the MOSFETs.

More specifically, when the accumulated charge is present in the channel regions of the off-state SOI MOSFETs **260***a*-**260***e* it responds to variations in the RF signals applied to their respective drains. As the time varying RF signal propagates along the transmission path **256**, the RF signal applies time varying source-to-drain bias voltages to the SOI MOSFETs **260***a*-**260***e*. The time varying source-to-drain bias voltages creates movement of the accumulated charge within the channel regions of the SOI MOSFETs **260**-**260***e*. The movement of the accumulated charge within the channel regions of the SOI MOSFETs causes variations in the drain-to-source off-state capacitance of the SOI MOSFETs **260***a*-**260***e*. More specifically, the movement of the accumulated charge within the channel regions causes a voltage dependence of the drain-to-source off-state capacitance as described above with reference to FIG. **2**A. The voltage dependent variations in the off-state capacitance of the SOI MOSFETs **260***a*-**260***e* is the dominant cause of harmonic distortion and IMD of the RF signal as it propagates through the RF switch **250**.

As noted above, harmonic distortion and IMD of the RF signal is a major disadvantage of the prior art RF switch circuits implemented using the prior art SOI MOSFET devices. For many applications, harmonics and IMD of the RF signal must be suppressed to levels that heretofore have been difficult or impossible to achieve using prior art SOI MOSFET devices. In GSM devices, for example, at a maximum operating power of +35 dBm, prior art switches typically have only a 6 dB margin to the GSM third order harmonics suppression requirement of less than −30 dBm. Very low even order harmonic distortion is also desirable in GSM systems as the second order harmonic of the GSM transmit band also resides in the DCS receive band. Suppression of odd order (e.g., third order) harmonics of the RF signal, however, is desirable and improvements in that regard are needed.

In addition, as is well known, presence of an accumulated charge in the bodies of floating body (e.g., SOI) MOSFETs can also adversely affect the drain-to-source breakdown voltage (BVDSS) performance characteristics of the floating body MOSFETs. As is well known, floating-body FETs demonstrate drain-to-source breakdown voltage problems, also known as BVDSS, wherein the drain-to-source "punch-through" voltage is reduced by a parasitic bipolar action. The parasitic bipolar action is caused when holes are generated in the channel and the holes have nowhere to dissipate (i.e., because the body is floating, the holes have no means for escaping the body). As a consequence, the potential of the MOSFET body is increased, which effectively reduces the threshold voltage. In turn, this condition causes the MOSFET device to experience increased leakage, thereby generating more holes in the body, and thereby exacerbating the BVDSS problem (as a result of this positive feedback condition).

The present disclosed method and apparatus for improving linearity of SOI (and SOS) MOSFET devices overcomes the above-described disadvantages of the prior art. Once the accumulated charge is recognized as a major source of harmonic distortion, IMD and compression/saturation in off-state SOI MOSFET devices, and in circuits (such as RF circuits) implemented with these devices, it becomes clear that reduction, removal, and/or control of the accumulated charge improves the harmonic suppression characteristics of these devices. In addition, reduction, removal, and/or control of the accumulated charge also improve the BVDSS performance characteristics by preventing the parasitic bipolar action from occurring. Improvements in BVDSS lead to consequent improvements in device linearity. Several exemplary structures and techniques for controlling the accumulated charge in SOI MOSFETs are described in detail in the next section.

Method and Apparatus for Improving the Linearity of MOSFETs Using Accumulated Charge Sinks (ACS)—Overview

As described below in more detail, the present disclosure describes methods and apparatuses for improving semiconductor device linearity (e.g., reducing adverse harmonic distortion and IMD effects) in SOI MOSFETs. In one exemplary embodiment, the method and apparatus improves the linearity and controls the harmonic distortion and IMD effects of the MOSFET devices by reducing the accumulated charge in the bodies of the MOSFET devices. In one embodiment, the present method and apparatus reduces or otherwise controls the accumulated charge in the MOSFET bodies using an accumulated charge sink (ACS) that is operatively coupled to the MOSFET body. In one embodiment, the present method and apparatus entirely removes all of the accumulated charge from the bodies of the MOSFET devices. In one described embodiment, the MOSFET is biased to operate in an accumulated charge regime, and the ACS is used to entirely remove, reduce, or otherwise control, the accumulated charge and thereby reduce harmonic distortions and IMD that would otherwise result. Linearity is also improved in some embodi-

ments by removing or otherwise controlling the accumulated charge thereby improving the floating body MOSFET BVDSS characteristics.

As noted in the background section above, persons skilled in the electronic device design and manufacture arts shall appreciate that the teachings herein apply equally to MOSFETs fabricated on Semiconductor-On-Insulator ("SOI") and Semiconductor-On-Sapphire ("SOS") substrates. The present teachings can be used in the implementation of MOSFETs using any convenient semiconductor-on-insulator technology. For example, the inventive MOSFETs described herein can be implemented using compound semiconductors fabricated on insulating substrates, such as GaAs MOSFETs. As noted above, the present method and apparatus may also be applied to silicon-germanium (SiGe) SOI MOSFETs. For simplicity, the embodiments and examples presented herein for illustrative purposes include only NMOSFETs, unless otherwise noted. By making well known changes to dopants, charge carriers, polarity of bias voltages, etc., persons skilled in the electronic device design arts will easily understand how these embodiments and examples may be adapted for use with PMOSFETs.

As noted above, the present disclosure is particularly applicable to FETs and associated applications benefiting from a fully depleted channel when the FET is operated in the off-state, wherein an accumulated charge may result. The disclosed method and apparatus for use in improving the linearity of MOSFETs also finds applicability for use with partially depleted channels. As known to those skilled in the art, the doping and dimensions of the body vary widely. In an exemplary embodiment, the body comprises silicon having a thickness of approximately 100 angstroms to approximately 2,000 angstroms. In a further exemplary embodiment, dopant concentration within the FET bodies ranges from no more than that associated with intrinsic silicon to approximately 1×10^{18} active dopant atoms per cm^3, resulting in fully-depleted transistor operation. In a further exemplary embodiment, dopant concentration within the FET bodies ranges from 1×10^{18} to 1×10^{19} active dopant atoms per cm^3 and/or the silicon comprising the body ranges from a thickness of 2000 angstroms to many micrometers, resulting in partially-depleted transistor operation. As will be appreciated by those skilled in the electronic design and manufacturing arts, the present disclosed method and apparatus for use in improving linearity of MOSFETs can be used in MOSFETs implemented in a wide variety of dopant concentrations and body dimensions. The present disclosed method and apparatus therefore is not limited for use in MOSFETs implemented using the exemplary dopant concentrations and body dimensions as set forth above.

According to one aspect of the present disclosure, accumulated charge within a FET body is reduced using control methodologies and associated circuitry. In one embodiment all of the accumulated charge is removed from the FET body. In other embodiments, the accumulated charge is reduced or otherwise controlled. In one embodiment, holes are removed from the FET body, whereas in another embodiment, electrons are removed from the FET body, as described below in more detail. By removing holes (or electrons) from the FET body using the novel and nonobvious teachings of the present disclosure, voltage induced variations in the parasitic capacitances of the off-state FETs are reduced or eliminated, thereby reducing or eliminating nonlinear behavior of the off-state FETs. In addition, as described above with reference to FIG. **2**A, because the body impedance is greatly increased when the accumulated charge is reduced or controlled, there is a beneficial overall reduction in the magnitude of the FET off-state capacitances. Also, as described above, removing or otherwise controlling the accumulated charge in floating body MOSFETs improves the BVDSS characteristics of the FET and thereby improves the linearity of the floating body MOSFET.

Accumulated charge control not only facilitates a beneficial overall reduction in the FET off-state capacitance C_{off} (as described above with reference to FIG. **2**A and below with reference to FIG. **4**H), it also facilitates a reduction in C_{off} variations that can occur over time in the presence of a time varying V_{ds} bias voltage. Thus, a reduction of undesirable harmonics generation and intermodulation distortion in RF switch circuits is obtained using SOI MOSFETs made in accordance with the present disclosure. Improved SOI MOSFET power handling, linearity, and performance are achieved by devices made in accordance with the present teachings. While the methods and apparatuses of the present disclosure are capable of fully removing accumulated charge from the FET bodies, those skilled in the electronic device design arts shall appreciate that any reduction of accumulated charge is beneficial.

Reductions in harmonics and intermodulation distortion are generally beneficial in any semiconductor system, either bulk semiconductor or semiconductor-on-insulator (SOI) systems. SOI systems include any semiconductor architecture employing semiconductor-containing regions positioned above an underlying insulating substrate. While any suitable insulating substrate can be used in a SOI system, exemplary insulating substrates include silicon dioxide (e.g., a buried oxide layer supported by a silicon substrate, such as that known as Separation by Implantation of Oxygen (SIMOX)), bonded wafer (thick oxide), glass, and sapphire. As noted above, in addition to the commonly used silicon-based systems, some embodiments of the present disclosure may be implemented using silicon-germanium (SiGe), wherein the SiGe is used equivalently in place of Si.

A wide variety of ACS implementations and structures can be used to practice the present disclosed method and apparatus. In accordance with one embodiment of the present method and apparatus, an ACS is used to remove or otherwise control accumulated charge (referenced as **120** in FIG. **1** described above) from the MOSFETs when the MOSFETs are configured to operate in the accumulated charge regime. By adapting the SOI (or SOS) MOSFETs in accordance with the present teachings, improved Accumulated Charge Control (ACC) MOSFETs are realized. The ACC MOSFETs are useful in improving performance of many circuits, including RF switching circuits. Various characteristics and possible configurations of the exemplary ACC MOSFETs are described in detail below with reference to FIGS. **3**A-**3**K. This section also describes how the exemplary ACS implementations of the present disclosure differ from the body contacts of the prior art.

The ACC MOSFET is shown schematically embodied as a four-terminal device in FIG. **4**A. FIGS. **4**B-**4**G show various exemplary simple circuit configurations that can be used in removing the accumulated charge from the ACC MOSFET when it operates in an accumulated charge regime. The operation of the simplified circuit configurations is described in more detail below with reference to FIGS. **4**A-**4**G. The improvement in off-state capacitance C_{off} of the ACC MOSFETs, as compared with the off-state capacitance of the prior art SOI MOSFETs, is described below with reference to FIG. **4**H.

The operation of various exemplary RF switch circuits implemented using the ACC MOSFETs of the present disclosure is described below with reference to the circuit schemat-

ics of FIGS. 5B-5D. Further, an exemplary RF switch circuit using stacked ACC MOSFETs (for increased power handling) of the present disclosure is described below with reference to FIG. 6. An exemplary method of improving the linearity of an SOI MOSFET using an accumulated charge sink (ACS) is described with reference to FIG. 7. Finally, exemplary fabrication methods that may be used to manufacture the ACC MOSFET are described. The various exemplary ACS implementations and structures that can be used to practice the disclosed method and apparatus are now described with reference to FIGS. 3A-3K.

Controlling Accumulated Charge Using an Accumulated Charge Sink (ACS)

FIGS. 3A and 3B are simplified schematic diagrams of a top view of an Accumulated Charge Control (ACC) SOI NMOSFET **300** adapted to control accumulated charge **120** (FIG. **1**) in accordance with the present disclosure. In the exemplary embodiment, a gate contact **301** is coupled to a first end of a gate **302**. A gate oxide (not shown in FIG. 3A but shown in FIG. 1) and a body **312** (shown in FIG. 3B) are positioned under the gate **302**. In the exemplary NMOSFET **300** shown, a source **304** and a drain **306** comprise N+ regions. In the exemplary embodiment, the ACC NMOSFET **300** includes an accumulated charge sink (ACS) **308** comprising a P− region. The ACS **308** is coupled to and is in electrical communication with the body **312** which also comprises a P− region. An electrical contact region **310** provides electrical connection to the ACS **308**. In some embodiments, the electrical contact region **310** comprises a P+ region. As shown in FIG. 3A, the electrical contact region **310** is coupled to and is in electrical communication with the ACS **308**.

Those skilled in the arts of electronic devices shall understand that the electrical contact region **310** may be used to facilitate electrical coupling to the ACS **308** because in some embodiments it may be difficult to make a direct contact to a lightly doped region. In addition, in some embodiments the ACS **308** and the electrical contact region **310** may be coextensive. In another embodiment, the electrical contact region **310** comprises an N+ region. In this embodiment, the electrical contact region **310** functions as a diode connection to the ACS **308**, which prevents positive current flow into the ACS **308** (and also prevents positive current flow into the body **312**) under particular bias conditions, as described below in more detail.

FIG. 3B is an alternative top view of the ACC SOI NMOSFET **300** of FIG. 3A, illustrating the ACC NMOSFET **300** without its gate contact **301**, gate **302**, and gate oxide being visible. This view allows the body **312** to be visible. FIG. 3B shows the coupling of the ACS **308** to one end of the body **312**. In one embodiment, the body **312** and the ACS **308** comprise a combined P− region that may be produced by a single ion-implantation step. In another embodiment, the body **312** and ACS **308** comprise separate P− regions that are coupled together.

As is well known to those skilled in the electronic device design arts, in other embodiments, the ACC NMOSFET **300** of FIGS. 3A and 3B can be implemented as an ACC PMOSFET simply by reversing the dopant materials used to implement the various FET component regions (i.e., replace p-type dopant material with n-type dopant material, and vice versa). More specifically, in an ACC PMOSFET, the source and drain comprise P+ regions, and the body comprises an N− region. In this embodiment, the ACS **308** also comprises an N− region. In some embodiments of the ACC PMOSFET, the electrical contact region **310** may comprise an N+ region. In other embodiments of the ACC PMOSFETs, the region **310** comprises a P+ region, which functions as a diode connection to the ACS **308** and thereby prevents current flow into the ACS **308** under particular bias conditions.

Prior Art Body Contacts Distinguished from the Disclosed ACS

According to the present disclosure, the ACS **308** used to implement ACC SOI MOSFETs includes novel features in structure, function, operation and design that distinguish it from the so-called "body contacts" (also sometimes referred to as "body ties", usually when the "body contact" is directly connected to the source) that are well known in the prior art.

Exemplary references relating to body contacts used in prior art SOI MOSFETs include the following: (1) F. Hameau and O. Rozeau, Radio-Frequency Circuits Integration Using CMOS SOI 0.25 μm Technology," 2002 RF IC Design Workshop Europe, 19-22 Mar. 2002, Grenoble, France; (2) J. R. Cricci et al., "Silicon on Sapphire MOS Transistor," U.S. Pat. No. 4,053,916, Oct. 11, 1977; (3) O. Rozeau et al., "SOI Technologies Overview for Low-Power Low-Voltage Radio-Frequency Applications," Analog Integrated Circuits and Signal Processing, 25, pp. 93-114, Boston, Mass., Kluwer Academic Publishers, November 2000; (4) C. Tinella et al., "A High-Performance CMOS-SOI Antenna Switch for the 2.5-5-GHz Band, "IEEE Journal of Solid-State Circuits, Vol. 38, No. 7, July, 2003; (5) H. Lee et al., "Analysis of body bias effect with PD-SOI for analog and RF applications," Solid State Electron., Vol. 46, pp. 1169-1176, 2002; (6) J.-H. Lee, et al., "Effect of Body Structure on Analog Performance of SOI NMOSFETs," Proceedings, 1998 IEEE International SOI Conference, 5-8 October 1998, pp. 61-62; (7) C. F. Edwards, et al., The Effect of Body Contact Series Resistance on SOI CMOS Amplifier Stages," IEEE Transactions on Electron Devices, Vol. 44, No. 12, December 1997 pp. 2290-2294; (8) S. Maeda, et al., Substrate-bias Effect and Source-drain Breakdown Characteristics in Body-tied Short-channel SOI MOSFET's," IEEE Transactions on Electron Devices, Vol. 46, No. 1, January 1999 pp. 151-158; (9) F. Assaderaghi, et al., "Dynamic Threshold-voltage MOSFET (DTMOS) for Ultra-low Voltage VLSI," IEEE Transactions on Electron Devices, Vol. 44, No. 3, March 1997, pp. 414-422; (10) G. 0. Workman and J. G. Fossum, "A Comparative Analysis of the Dynamic Behavior of BTG/SOI MOSFETs and Circuits with Distributed Body Resistance," IEEE Transactions on Electron Devices, Vol. 45, No. 10, October 1998 pp. 2138-2145; and (11) T.-S. Chao, et al., "High-voltage and High-temperature Applications of DTMOS with Reverse Schottky Barrier on Substrate Contacts," IEEE Electron Device Letters, Vol. 25, No. 2, February 2004, pp. 86-88.

As described herein, applications such as RF switch circuits, may use SOI MOSFETs operated with off-state bias voltages, for which accumulated charge may result. The SOI MOSFETs are defined herein as operating within the accumulated charge regime when the MOSFETs are biased in the off-state, and when carriers having opposite polarity to the channel carriers are present in the channel regions of the MOSFETs. In some embodiments, the SOI MOSFETs may operate within the accumulated charge regime when the MOSFETs are partially depleted yet still biased to operate in the off-state. Significant benefits in improving nonlinear effects on source-drain capacitance can be realized by removing or otherwise controlling the accumulated charge according to the present teachings. In contrast to the disclosed techniques, none of the cited prior art teach or suggest ACS methods and apparatuses that are uniquely useful for removing or controlling accumulated charge. Nor are they informed regarding problems caused by the accumulated charge such as nonlinear effects on the off-state source-drain capacitance C_{off}. Consequently, the prior art body contacts described in

the references cited above differ greatly (in structure, function, operation and design) from the ACSs described with reference to FIGS. **3**A-**4**D.

In one example, the ACS **308** operates effectively to remove or otherwise control the accumulated charge from the SOI NMOSFET **300** using a high impedance connection to and throughout the body **312**. High impedance ACSs may be used because the accumulated charge **120** is primarily generated by phenomena (e.g., thermal generation) that take a relatively long period of time to produce significant accumulated charge. For example, a typical time period for producing non-negligible accumulated charge when the NMOSFET operates in the accumulated charge regime is approximately a few milliseconds or greater. Such relatively slow generation of accumulated charge corresponds to very low currents, typically less than 100 nA/mm of transistor width. Such low currents can be effectively conveyed even using very high impedance connections to the body. According to one example, the ACS **308** is implemented with a connection having a resistance of greater than 10^6 ohms. Consequently, the ACS **308** is capable of effectively removing or otherwise controlling the accumulated charge **120** even when implemented with a relatively high impedance connection, relative to the low impedance prior art body contacts.

In stark contrast, the prior art teachings of body contacts described in the references cited above require low impedance (high efficiency) access to the body regions of SOI MOSFETs for proper operation (see, e.g., references (3), (6), and (7) above). A principal reason for this requirement is that the prior art body contacts are primarily directed to reducing the adverse effects on SOI MOSFET functions caused by much faster and more effective electron-hole pair generation processes than occur when the FET is operated in the accumulated charge regime. For example, in some prior art MOSFETs not operated in the accumulated charge regime, electron-hole pair carriers are generated as a result of impact ionization. Impact ionization produces electron-hole pairs at a much faster rate than occurs when the FET is operated in the accumulated charge regime.

The relative rates for electron-hole pair generation by impact ionization versus the pair generation processes causing accumulated charge can be estimated from the roll-off frequencies for the two phenomena. For example, reference (3) cited above indicates roll-off frequencies for impact ionization effects in the range of 10^5 Hz. In contrast, a roll-off frequency for the accumulated charge effects has been observed to be in the range of 10^3 Hz or less, as indicated by recovery times for odd harmonics. These observations indicate that the ACS **308** can effectively control accumulated charge using an impedance that is at least 100 times larger than required of prior art body contacts used in controlling impact ionization charge, for example. Further, because impact ionization primarily occurs when the SOI MOSFET operates in an on-state, the effects of impact ionization can be amplified by on-state transistor operation. Low impedance body contacts to and throughout a body region is even more critical in these environments in order to control the effects of impact ionization under the on-state conditions.

In stark contrast, the ACS **308** of the present teachings removes or otherwise controls the accumulated charge only when the ACC SOI MOSFET operates in the accumulated charge regime. By definition, the FET is in the off-state in this regime, so there is no requirement to remove impact ionization as amplified by an on-state FET. Therefore, a high impedance ACS **308** is perfectly adequate for removing the accumulated charge under these operating conditions. The prior art requirements for low impedance body connections results in numerous problems of implementation that are overcome by the present teachings, as described below in more detail.

In addition, the ACS **308** may be implemented with much lower source-to-drain parasitic capacitance as compared to the body contacts of the prior art. The above-described low impedance connection to the SOI MOSFET body required of the prior art body contacts necessitates proximity of the contacts to the entire body. This may require a plurality body contact "fingers" that contact the body at different locations along the body. The low impedance connection to the body also necessitates proximity of the prior art body contacts to the source and drain. Because of parasitic capacitances produced by such body contacts, the cited prior art references teach away from the use of such structures for many high frequency applications such as RF. In stark contrast, the ACS **308** of the present disclosure may be positioned a selected distance away from the source **304** and the drain **306**, and the ACS **308** may also be coupled to the body **312** at a first distal end of the body **312** (shown in FIGS. **3**A and **3**B). Arranged in this manner, the ACS **308** makes minimal contact (as compared to the prior art body contacts that may contact the body at many locations along the body) with the body **312**. This configuration of the ACS **308** with the MOSFET eliminates or greatly reduces the parasitic capacitances caused by a more proximate positioning of the ACS **308** relative to the source, drain, and body. Further, the ACS **308** may be implemented in SOI MOSFETs operated with a depleted channel. In general, the cited prior art references teach away from the use of body contacts for this environment (see, e.g., reference (3), cited above).

Further, because impact ionization hole currents are much larger (in the range of 5,000 nA per mm body width) than for accumulated charge generation (less than approximately 100 nA per mm body width), the prior art does not teach how to effectively implement very large body widths (i.e., much greater than approximately 10 μm). In contrast, the ACS **308** of the present disclosed device may be implemented in SOI MOSFETs having relatively large body widths. This provides improvements in on-state conductance and transconductance, insertion loss and fabrication costs, particularly for RF switch devices. According to the prior art teachings cited above, larger body widths adversely affect the efficient operation of body contacts because their impedances are necessarily thereby increased. Although the cited prior art suggests that a plurality of fingers may be used to contact the body at different locations, the plurality of fingers adversely affects parasitic source-to-drain capacitances, as described above.

For these reasons, and for the reasons described below in more detail, the present disclosure provides novel MOSFET devices, circuits and methods that overcome the limitations according to the prior art teachings as cited above.

FIG. **3**C is a cross-sectional perspective schematic of an ACC SOI NMOSFET **300'** adapted to control accumulated charge in accordance with the disclosed method and apparatus. In the example shown in FIG. **3**C, the ACC NMOSFET **300'** includes four terminals that provide electrical connection to the various FET component regions. In one embodiment, the terminals provide means for connecting external integrated circuit (IC) elements (such as metal leads, not shown) to the various FET component regions. Three of the terminals shown in FIG. **3**C are typically available in prior art FET devices. For example, as shown in FIG. **3**C, the ACC NMOSFET **300'** includes a gate terminal **302'** that provides electrical connection to the gate **302**. Similarly, the ACC NMOSFET **300'** includes source and drain terminals **304'**, **306'** that provide electrical connection to the source **304** and drain **306**, respectively. As is well known in the electronic

design arts, the terminals are coupled to their respective FET component regions (i.e., gate, drain and source) via so-called "ohmic" (i.e., low resistance) contact regions. The manufacturing and structural details associated with the coupling of the various FET terminal to the FET component regions are well known in the art, and therefore are not described in more detail here.

As described above with reference to FIGS. **3**A and **3**B, the ACC NMOSFET **300'** is adapted to control accumulated charge when the NMOSFET operates in the accumulated charge regime. To this end, in the exemplary embodiment shown in FIG. **3**C, the ACC NMOSFET **300'** includes a fourth terminal that provides electrical connection to the body **312**, and thereby facilitates reduction (or other control) of the accumulated charge when the FET **300'** operates in the accumulated charge regime. More specifically, and referring again to FIG. **3**C, the ACC NMOSFET includes a "body" terminal, or Accumulated Charge Sink (ACS) terminal **308'**. The ACS terminal **308'** provides an electrical connection to the ACS **308** (not shown in FIG. **3**C, but shown in FIGS. **3**A and **3**B) and to the body **312**. Although the ACS terminal **308'** is shown in FIG. **3**C as being physically coupled to the body **312**, those skilled in the electronic design arts shall understand that this depiction is for illustrative purposes only. The direct coupling of the ACS terminal **308'** to the body **312** shown in FIG. **3**C illustrates the electrical connectivity (i.e., not the physical coupling) of the terminal **308'** with the body **312**. Similarly, the other terminals (i.e., terminals **302'**, **304'** and **306'**) are also shown in FIG. **3**C as being physically coupled to their respective FET component regions. These depictions are also for illustrative purposes only.

In most embodiments, as described above with reference to FIGS. **3**A-**3**B, and described further below with reference to FIGS. **3**D-**3**K, the ACS terminal **308'** provides the electrical connection to the body **312** via coupling to the ACS **308** via the electrical contact region **310**. However, the present disclosure also contemplates embodiments where the coupling of the ACS terminal **308'** is made directly to the body **312** (i.e., no intermediate regions exist between the ACS terminal **308'** and the body **312**).

In accordance with the disclosed method and apparatus, when the ACC NMOSFET **300'** is biased to operate in the accumulated charge regime (i.e., when the ACC NMOSFET **300'** is in the off-state, and there is an accumulated charge **120** of P polarity (i.e., holes) present in the channel region of the body **312**), the accumulated charge is removed or otherwise controlled via the ACS terminal **308'**. When accumulated charge **120** is present in the body **312**, the charge **312** can be removed or otherwise controlled by applying a bias voltage (V_b (for "body") or V_{ACS} (ACS bias voltage)) to the ACS terminal **308'**. In general, the ACS bias voltage V_{ACS} applied to the ACS terminal **308'** may be selected to be equal to or more negative than the lesser of the source bias voltage Vs and drain bias voltage Vd. More specifically, in some embodiments, the ACS terminal **308'** can be coupled to various accumulated charge sinking mechanisms that remove (or "sink") the accumulated charge when the FET operates in the accumulated charge regime. Several exemplary accumulated charge sinking mechanisms and circuit configurations are described below with reference to FIGS. **4**A-**5**D.

Similar to the prior art NMOSFET **100** described above with reference to FIG. **1**, the ACC SOI NMOSFET **300'** of FIG. **3**C can be biased to operate in the accumulated charge regime by applying specific bias voltages to the various terminals **302'**, **304'**, and **306'**. In one exemplary embodiment, the source and drain bias voltages (Vs and Vd, respectively) are zero (i.e., the terminals **304'** and **306'** are connected to ground). In this example, if the gate bias voltage (Vg) applied to the gate terminal **302'** is sufficiently negative with respect to the source and drain bias voltages, and with respect to V_{th} (for example, if V_{th} is approximately zero, and if Vg is more negative than approximately −1 V), the ACC NMOSFET **300'** operates in the off-state. If the ACC NMOSFET **300'** continues to be biased in the off-state, the accumulated charge (holes) will accumulate in the body **312**. Advantageously, the accumulated charge can be removed from the body **312** via the ACS terminal **308'**. In some embodiments, as described below in more detail with reference to FIG. **4**B, the ACS terminal **308'** is coupled to the gate terminal **302'** (thereby ensuring that the same bias voltages are applied to both the gate (Vg) and the body (shown in FIG. **3**C as "Vb" or "V_{ACS}").

However, those skilled in the electronics design arts shall appreciate that a myriad of bias voltages can be applied to the four device terminals while still employing the techniques of the present disclosed method and apparatus. As long as the ACC SOI NMOSFET **300'** is biased to operate in the accumulated charge regime, the accumulated charge can be removed or otherwise controlled by applying a bias voltage V_{ACS} to the ACS terminal **308'**, and thereby remove the accumulated charge from the body **312**.

For example, in one embodiment wherein the ACC NMOSFET **300'** comprises a depletion mode device, V_{th} is negative by definition. In this embodiment if both the Vs and Vd bias voltages comprise zero volts (i.e., both terminals tied to circuit ground node), and a gate bias Vg applied to the gate terminal **302'** is sufficiently negative to V_{th} (for example, Vg is more negative than approximately −1 V relative to V_{th}), holes may accumulate under the gate oxide **110** thereby becoming the accumulated charge **120**. In this example, in order to remove the accumulated holes (i.e., the accumulated charge **120**) from the FET body **312**, the voltage V_{ACS} applied to the ACS **308** may be selected to be equal to or more negative than the lesser of Vs and Vd.

In other examples, the source and drain bias voltages, Vs and Vd, respectively, may comprise voltage other than zero volts. According to these embodiments, the gate bias voltage Vg must be sufficiently negative to both Vs and Vd (in order for Vg to be sufficiently negative to V_{th}, for example) in order to bias the NMOSFET in the off-state. As described above, if the NMOSFET is biased in the off-state for a sufficiently long time period (approximately 1-2 ms, for example) an accumulated charge will accumulate under the gate oxide. In these embodiments, as noted above, in order to remove the accumulated charge **120** from the body **312**, the ACS bias voltage V_{ACS} applied to the ACS terminal **308'** may be selected to be equal to or more negative than the lesser of Vs and Vd.

It should be noted that, in contrast to the examples described above, the prior art body contacts are implemented largely for purposes of mitigating the adverse effects caused by impact ionization. Consequently, the prior art body contacts are typically tied to the source of the MOSFET. In order to effectively control, reduce, or entirely remove the accumulated charge in an NMOSFET, V_{ACS} should, in the exemplary embodiments, be equal to or more negative than the lesser of Vs and Vd. Those skilled in the electronic device design arts shall appreciate that different Vs, Vd, Vg and V_{ACS} bias voltages may be used when the ACC MOSFET comprises a PMOSFET device. Because the prior art body contacts are typically tied to the source, this implementation cannot be effected using the prior art body contact approach.

FIG. **3**D is a simplified schematic diagram of a top view of an ACC SOI NMOSFET **300"** adapted to control accumulated charge **120** (FIG. **1**) in accordance with the present

disclosure. FIG. **3**D shows the ACC NMOSFET **300"** without its gate contact **301**, gate **302**, and gate oxide being visible. The ACC NMOSFET **300"** of FIG. **3**D is very similar in design to the ACC NMOSFET **300** described above with reference to FIGS. **3**A and **3**B. For example, similar to the ACC NMOSFET **300**, the ACC NMOSFET **300"** includes a source **304** and drain **306** comprising N+ regions. The ACC NMOSFET **300"** also includes an accumulated charge sink (ACS) **308** comprising a P− region. As shown in FIG. **3**D, the P− region that comprises the ACS **308** abuts (i.e., is directly adjacent) the body **312**, which also comprises a P− region. Similar to the ACC NMOSFET **300**, the ACC NMOSFET **300"** includes an electrical contact region **310** that provides electrical connection to the ACS **308**. As noted above, in some embodiments, the electrical contact region **310** comprises a P+ region. In another embodiment, the electrical contact region **310** may comprise an N+ region (which thereby prevents positive current flow into the body **312** as noted above). As shown in FIG. **3**D, the electrical contact region **310** is formed in the ACC NMOSFET **300"** directly adjacent the ACS **308**. The ACC SOI NMOSFET **300"** functions to control accumulated charge similarly to the operation of the ACC NMOSFETs described above with reference to FIGS. **3**A-**3**C.

FIG. **3**E is a simplified schematic diagram of a top view of an ACC SOI NMOSFET **300'"** adapted to control accumulated charge in accordance with the present disclosure. The ACC NMOSFET **300'"** is very similar in design and function to the ACC NMOSFETs described above with reference to FIGS. **3**A-**3**D. FIG. **3**E shows a dashed cross-sectional view line A-A' taken along the approximate center of the NMOSFET **300'"**. This cross-sectional view is used herein to describe structural and performance characteristics of some exemplary prior art MOSFETS and some embodiments of the ACC NMOSFET that may occur as a result of the fabrication processes. Details of this cross-sectional view A-A' are now described with reference to FIG. **3**F.

View line A-A' slices through the following component regions of the ACC NMOSFET **300'"**: the P+ electrical contact region **310**, the ACS **308** (shown in FIG. **3**E, but not shown in FIG. **3**F), a P+ overlap region **310'**, a gate oxide **110**, and a poly-silicon gate **302**. In some embodiments, during the fabrication process, when the region **310** is doped with p-type dopant material, proximate the P− body region, some additional P+doping may be implanted (i.e., the p-type dopant material may overlap) into the P+ overlap region **310'** of the poly-silicon gate **302**. In some embodiments, such overlapping is performed intentionally to ensure that all of the gate oxide **110** is completely covered by the P+ region (i.e., to ensure that no gap exists on the edge of the oxide **110** between the gate **302** and the P+ region **310**). This, in turn, aids in providing a minimum impedance connection between the P+ region **310** and the body **312**.

Although the present teachings encompass such embodiments described above, those skilled in the electronic device design and manufacturing arts shall recognize that such low-resistance connections are not required. Therefore, disadvantages associated with the embodiment shown in FIG. **3**H, as described below in more detail, can be overcome by using other embodiments described herein (for example, the embodiments **300** and **300'"** described below with reference to FIGS. **3**G and **3**J, respectively), in which gaps are intentionally implemented between the P+ region **310** and the body **312**. In one exemplary embodiment, the P+overlap region **310'** overlaps the oxide **110** by approximately 0.2-0.7 microns. Those skilled in the MOSFET design and manufacturing arts shall appreciate that other overlap region dimensions can be used in practicing the present disclosed method and apparatus. In some embodiments, as shown in FIG. **3**F, for example, the remaining area over the gate oxide **110** and over the P− body is doped with n-type dopant material (i.e., it comprises an N+ region).

Referring again to FIG. **3**F, owing to the presence of the P+ overlap region **310'** over the gate oxide **110**, over the body **312**, and proximate an edge **340** of the poly-silicon gate **302**, an increased threshold voltage region is created in the NMOSFET **300'"**. More specifically, due to the P+ doping (in the P+ overlap region **310'**) proximate the edge **340** of the gate **302** over the channel region of the body **312**, a region of increased threshold voltage is formed in that region of the MOSFET **300'"**. The effects of the region of increased threshold voltage are now described in more detail with reference to FIGS. **3**H and **3**I.

FIG. **3**I shows a plot **380** of inversion channel charge versus applied gate voltage for an ACC NMOSFET. The plot **380** shown in FIG. **3**I illustrates one effect of the above-described increased threshold voltage that can occur in prior art MOSFETs, and in some embodiments of the present ACC NMOSFETs due to certain manufacturing processes. As described in more detail below, the increased threshold voltage region, shown in FIG. **3**H and described in more detail below, also occurs in prior art MOSFET designs due to the proximity of body ties to the FET body. As described below in more detail with reference to FIG. **3**J, for example, the present disclosed method and apparatus can be used to reduce or eliminate the region of increased threshold voltage found in some prior art SOI MOSFET designs.

FIG. **3**H shows one embodiment of an ACC NMOSFET without its gate contact, gate, and gate oxide being visible. The MOSFET region of increased threshold voltage described above with reference to FIGS. **3**E and **3**F is shown in FIG. **3**H as occurring in the region encompassed by the ellipse **307**. As will be well understood by those skilled in the electronic design and manufacturing arts, for the reasons set forth above with reference to FIGS. **3**E and **3**F, due to the increased threshold voltage, the region **307** of the ACC MOSFET shown in FIG. **3**H effectively "turns on" after the rest of the ACC MOSFET channel region.

The increased threshold voltage can be reduced by reducing the size of the region **307**. Eliminating the region **307** altogether eliminates the threshold voltage increase. Because the threshold voltage increase can increase harmonic and intermodulation distortion of the "on" state MOSFET, eliminating this effect improves MOSFET performance. The increased threshold voltage also has the detrimental effect of increasing the MOSFET on-resistance (i.e., the resistance presented by the MOSFET when it is in the on-state (conducting state), which detrimentally impacts the MOSFET insertion loss.

In one exemplary embodiment, as shown, for example in the embodiments of the ACC NMOSFET **300** described above with reference to FIGS. **3**A and **3**B, and as described below in more detail with reference to the cross-sectional view of the ACC MOSFET **300** of FIG. **3**G, the detrimental effects associated with threshold voltage increase are mitigated or overcome by positioning the P+ region **310** a selected distance away from an edge of the poly-silicon gate **302**. This approach is shown both in the top view of the ACC MOSFET **300** of FIG. **3**A, and in the cross-sectional view of the ACC MOSFET **300** shown in FIG. **3**G. As shown in the cross-sectional view of the ACC MOSFET **300** of FIG. **3**G, the P+ region **310** does not extend all the way to the edge **340** of the poly-silicon gate **302**. This is in stark contrast to the embodiment **300'"** shown in FIG. **3**F, where the P+ region **310'** extends all the way to the gate edge **340**. By positioning the

P+ region **310** a distance away from the gate edge **340** as shown in the embodiment **300** of FIG. **3**G, no P+ region is positioned proximate the poly-silicon gate **302** (i.e., there is no P+ region present in the poly-silicon gate **302**).

This configuration of the P+ region **310** eliminates or greatly reduces the problems associated with threshold voltage increase as described above. As described above with reference to FIGS. **3**A and **3**B, and with reference to the comparisons to the prior art body contact references, the relatively high impedance of the ACS **308** P– region (shown in FIG. **3**A) between the P+ region **310** and the gate **302** does not adversely affect the performance of the ACC NMOSFET **300**. As described above, the accumulated charge can be effectively removed even using a relatively high impedance ACS connection.

In another exemplary embodiment, as described below with reference to FIG. **3**J, the threshold voltage increase is removed by positioning the P+ region **310** (and the ACS **308**) a distance away from the body **312**. Because the electrical connectivity between the ACS **308** and the body **312** has relatively high impedance when the small region of P+ **310** is positioned a distance away from the body **312**, this approach is never taught or suggested by the body contact prior art references (which require low impedance contacts as described above). This improved embodiment is described next with reference to FIG. **3**J.

FIG. **3**J is a simplified top view schematic of another embodiment of an ACC SOI NMOSFET **300''''** adapted to control accumulated charge and configured in a "T-gate" configuration. FIG. **3**J shows the ACC NMOSFET **300''''** without its gate contact **301**, gate **302**, and gate oxide being visible. The gate (not shown in FIG. **3**J) and the body **312** are configured as "supporting" members of the "T-gate" configured ACC MOSFET **300''''** (i.e., they comprise the "bottom" portion of the "T-shaped" FET). These "supporting" members "support" the "supported" member of the T-gate configured MOSFET **300''''**, which comprises the ACS **308** as shown in FIG. **3**J (i.e., the ACS **308** comprises the "top" portion of the "T-shaped" FET). As shown in FIG. **3**J, the ACC NMOSFET **300''''** includes a small P+ region **310** conjoined to an ACS **308**. As shown in FIG. **3**J, the P+ region **310** (and thus the ACS external electrical connection) is disposed a selected distance away from the body **312**. The total impedance of the electrical connection from the body **312**, through the ACS **308**, and to the P+ region **310** is increased by positioning the P+ region **310** a selected distance away from the body **312**. However, as described above, the present ACC NMOSFET **300''''** works perfectly well to remove accumulated charge even using relatively high impedance ACS connections. For the reasons described above with reference to FIGS. **3**A and **3**B, due to the nature of the accumulated charge when the NMOSFET **300''''** operates in the accumulated charge regime, the ACC NMOSFET **300''''** does not require low impedance ACS electrical connections in order to remove accumulated charge from the body **312**. Rather, an ACS connection of relatively large impedance may be used in practicing the present teachings, with corresponding improvements in NMOSFET performance as described above (e.g., reductions in parasitic capacitance as compared with prior art low impedance body contacts). However, in other embodiments, if desired, a low impedance ACS connection may be used to practice the disclosed method and apparatus for use in improving linearity characteristics of SOI MOSFETs.

Moreover, as described above with reference to FIG. **3**H, the embodiment of FIG. **3**J improves device performance owing to the fact that the small P+ region **310** is positioned a distance away from the body **312**. Because the small P+ region **310** is positioned a distance away from the body **312**, the threshold voltage increase is reduced or entirely eliminated, together with the consequent adverse performance effects described above.

FIG. **3**K is a simplified top view schematic of another embodiment of an ACC SOI NMOSFET **300''''''** adapted to control accumulated charge and configured in an "H-gate" configuration. FIG. **3**K shows the ACC NMOSFET **300''''''** without its gate contact **301**, gate **302**, and gate oxide being visible. With the exception of some structural differences described herein, the ACC NMOSFET **300''''''** is very similar in design and function to the ACC NMOSFETs described above with reference to FIGS. **3**A-**3**D and **3**J. As shown in FIG. **3**K, the ACC NMOSFET **300''''''** includes two ACSs, **308** and **308''**, disposed at opposite ends of the H-gate ACC NMOSFET **300''''''**. P+ regions **310** and **310''** are formed to abut their respective ACSs, **308** and **308''**, and provide electrical contact thereto. In accordance with the disclosed method and apparatus, as described above, when the ACC NMOSFET **300''''''** is biased to operate in the accumulated charge regime, the accumulated charge is removed or otherwise controlled via the two ACSs **308** and **308''**.

It shall be understood by those skilled in the electronic device design arts that although the illustrated embodiment shows the ACSs **308** and **308''** extending approximately the entire width of the ACC NMOSFET **300''''''**, the ACSs **308** and **308''** may also comprise much narrower (or wider) regions, and still function perfectly well to remove or otherwise control the accumulated charge. Also, in some embodiments, it is not necessary that the impedance of the ACS **308** matches the impedance of the ACS **308''**. It will further be understood by the skilled person that the ACSs **308** and **308''** may comprise different sizes and configurations (i.e., rectangular, square, or any other convenient shape), and may also be positioned at various distances away from the body **312** (i.e., not necessarily the same distance away from the body **312**). As described above with reference to FIG. **3**J, when the ACS **308** is positioned a selected distance away from the body **312**, the problems associated with threshold voltage increase are reduced or eliminated.

Four-Terminal ACC MOSFET Devices—Simple Circuit Configurations

The SOI NMOSFET **300** of FIGS. **3**A and **3**B may be implemented as a four terminal device, as illustrated schematically in FIG. **4**A. As shown in the improved ACC SOI NMOSFET **300** of FIG. **4**A, a gate terminal **402** is electrically coupled to the gate contact **301** (e.g., FIG. **3**A) and is analogous to the gate terminal **302'** shown in FIG. **3**C. The gate contact **301** is electrically coupled to the gate **302** (e.g., FIGS. **3**A and **3**C). Similarly, a source terminal **404** is electrically coupled to the source **304** (e.g., FIGS. **3**A-**3**C) and is analogous to the source terminal **304'** of FIG. **3**C. Similarly, a drain terminal **406** is electrically coupled to the drain **306** (e.g., FIGS. **3**A-**3**C) and is analogous to the drain terminal **306'** of FIG. **3**C. Finally, the ACC NMOSFET **300** includes an ACS terminal **408** that is electrically coupled to the ACS **308** (e.g., see FIGS. **3**A-**3**B, and FIGS. **3**D, **3**J-**3**K) via the region **310**. Those skilled in the electronic design and manufacturing arts shall understand that the region **310** may be used in some embodiments to facilitate electrical coupling to the ACS **308** because, in some embodiments, it may be difficult to make a direct contact to a lightly doped region (i.e., the ACS **308**). The ACS terminal **408** is analogous to the ACS terminal **308'** shown in FIG. **3**C.

The ACC SOI NMOSFET **300** of FIG. **4**A may be operated using various techniques and implemented in various circuits in order to control accumulated charge present in the FET

when it is operating in an accumulated charge regime. For example, in one exemplary embodiment as shown in FIG. **4**B, the gate and ACS terminals, **402** and **408**, respectively, are electrically coupled together. In one embodiment of the simplified circuit shown in FIG. **4**B, the source and drain bias voltages applied to the terminals **404** and **406**, respectively, may be zero. If the gate bias voltage (Vg) applied to the gate terminal **402** is sufficiently negative with respect to the source and drain bias voltages applied to the terminals **404** and **406**, and with respect to the threshold voltage V_{th}, (for example, if V_{th} is approximately zero, and if Vg is more negative than approximately −1 V) the ACC NMOSFET **300** operates in the accumulated charge regime. As described above with reference to FIG. **3**C, for example, when the MOSFET operates in this regime, accumulated charge (holes) may accumulate in the body of the NMOSFET **300**.

Advantageously, the accumulated charge can be removed via the ACS terminal **408** by connecting the ACS terminal **408** to the gate terminal **402** as shown. This configuration ensures that when the FET **300** is in the off-state, it is held in the correct bias region to effectively remove or otherwise control the accumulated charge. As shown in FIG. **4**B, connecting the ACS terminal **408** to the gate ensures that the same bias voltages are applied to both the gate (Vg) and the body (shown in FIG. **3**C as "Vb" or "V_{ACS}"). Because the bias voltage V_{ACS} is the same as the gate voltage Vg in this embodiment, the accumulated charge is no longer trapped below the gate oxide (by attraction to the gate bias Vg) because it is conveyed to the gate terminal **402** via the ACS terminal **408**. The accumulated charge is thereby removed from the body via the ACS terminal **408**.

In other exemplary embodiments, as described above with reference to FIG. **3**C, for example, Vs and Vd may comprise nonzero bias voltages. According to these examples, Vg must be sufficiently negative to both Vs and Vd in order for Vg to be sufficiently negative to V_{th} to turn the NMOSFET **300** off (i.e., operate the NMOSFET **300** in the off-state). When so biased, as described above, the NMOSFET **300** may enter the accumulated charge regime and thereby have accumulated charge present in the body. For this example, the voltage V_{ACS} may also be selected to be equal to Vg by connecting the ACS terminal **408** to the gate terminal **402**, thereby conveying the accumulated charge from the body of the ACC NMOSFET, as described above.

In another exemplary embodiment, as described above, the ACC NMOSFET **300** comprises a depletion mode device. In this embodiment, the threshold voltage, V_{th} is, by definition, less than zero. For Vs and Vd both at zero volts, when a gate bias Vg sufficiently negative to V_{th} is applied to the gate terminal **402** (for example, Vg more negative than approximately −1 V relative to V_{th}), holes may accumulate under the gate oxide and thereby comprise an accumulated charge. For this example, the voltage V_{ACS} may also be selected to be equal to Vg by connecting the ACS terminal **408** to the gate terminal **402**, thereby conveying the accumulated charge from the ACC NMOSFET as described above.

In some embodiments of the improved ACC SOI NMOSFET **300**, such as that described above with reference to FIG. **4**B, when the FET is biased on, diodes formed at the edge of the device (such as described above with reference to the interface between the ACS **308** and the drain **304** (and the source **306**) as shown in FIG. **3**D) may become forward biased thereby allowing current to flow into the source and drain regions. In addition to wasting power, this may introduce nonlinearity into the NMOSFET. The nonlinearity results because the current that flows as a result of the forward biased interface diodes comprises nonlinear current. As Vgs and Vgd are reduced in that region of the device, the on resistance Ron at the edge of the device is increased. As is well known, and for the reasons set forth above, if the interface diodes formed at the edge of the device become forward biased, the device on-state characteristics are consequently dramatically adversely affected. Those skilled in the electronic device design arts shall understand that the configuration shown in FIG. **4**B limits application of a gate bias voltage Vgs to approximately 0.7 Volts. The simplified circuit shown in FIG. **4**C can be used to overcome these problems.

Another exemplary simplified circuit using the improved ACC SOI NMOSFET **300** is shown in FIG. **4**C. As shown in FIG. **4**C, in this embodiment, the ACS terminal **408** may be electrically coupled to a diode **410**, and the diode **410** may, in turn, be coupled to the gate terminal **402**. This embodiment may be used to prevent a positive current flow into the MOSFET body **312** caused by a positive Vg-to-Vs (or, equivalently, Vgs, where Vgs=Vg−Vs) bias voltage, as may occur, for example, when the SOI NMOSFET **300** is biased into an on-state condition.

As with the device shown in FIG. **4**B, when biased off, the ACS terminal voltage V_{ACS} comprises the gate voltage plus a voltage drop across the diode **410**. At very low ACS terminal current levels, the voltage drop across the diode **410** typically also is very low (e.g., <<500 mV, for example, for a typical threshold diode). The voltage drop across the diode **410** can be reduced to approximately zero by using other diodes, such as a 0 Vf diode, for example. In one embodiment, reducing the voltage drop across the diode is achieved by increasing the diode **410** width. Additionally, maintaining the ACS-to-source or ACS-to-drain voltage (whichever bias voltage of the two bias voltages is lower) increasingly negative, also improves the linearity of the ACC MOSFET device **300**.

When the SOI NMOSFET **300** is biased in an on condition, the diode **410** is reverse-biased, thereby preventing the flow of positive current into the source and drain regions. The reverse-biased configuration reduces power consumption and improves linearity of the device. The circuit shown in FIG. **4**C therefore works well to remove accumulated charge from the ACC MOSFET body when the FET is in the off-state and is operated in the accumulated charge regime. It also permits almost any positive voltage to be applied to the gate voltage Vg. This, in turn, allows the ACC MOSFET to effectively remove accumulated charge when the device operates in the off-state, yet assume the characteristics of a floating body device when the device operates in the on-state.

With the exception of the diode **410** used to prevent the flow of positive current into the ACS terminal **408**, exemplary operation of the simplified circuit shown in FIG. **4**C is the same as the operation of the circuit described above with reference to FIG. **4**B.

In yet another embodiment, the ACS terminal **408** may be coupled to a control circuit **412** as illustrated in the simplified circuit of FIG. **4**D. The control circuit **412** may provide a selectable ACS bias voltage V_{ACS} that selectively controls the accumulated charge (i.e., the accumulated charge **120** described above with reference to FIG. **1**). As shown in FIG. **4**D, rather than having a local circuit provide the ACS bias voltage V_{ACS} (e.g., as derived from the gate voltage Vg), in some embodiments the ACS bias voltage V_{ACS} is produced by a separate source that is independent of the ACC MOSFET device **300**. In the case of a switch (as described below in more detail with reference to FIG. **4**E), the ACS bias voltage V_{ACS} should be driven from a source having a high output impedance. For example, such a high output impedance source can be obtained using a large series resistor in order to ensure that the RF voltage is divided across the MOSFET and

that the ACS bias voltage V_{ACS} has Vds/2 "riding" on it, similarly to the gate voltage. This approach is described in more detail below with reference to FIG. **4**E.

It may be desirable to provide a negative ACS bias voltage V_{ACS} to the ACS terminal **408** when the SOI NMOSFET **300** is biased into an accumulated charge regime. In this exemplary embodiment, the control circuit **412** may prevent positive current flow into the ACS terminal **408** by selectively maintaining an ACS bias voltage V_{ACS} that is consistently negative with respect to both the source and drain bias voltages. In particular, the control circuit **412** may be used to apply an ACS bias voltage that is equal to or more negative than the lesser of Vs and Vd. By application of such an ACS bias voltage, the accumulated charge is thereby removed or otherwise controlled.

In the exemplary embodiment of the simplified circuit shown in FIG. **4**D, the source and drain bias voltages applied to the terminals **404** and **406**, respectively, may be zero. If the gate bias voltage (Vg) applied to the gate terminal **402** is sufficiently negative with respect to the source and drain bias voltages applied to the terminals **404** and **406**, and with respect to V_{th}, (for example, if V_{th} is approximately zero, and if Vg is more negative than approximately −1 V) the ACC NMOSFET **300** operates in the accumulated charge regime, and the accumulated charge (holes) may accumulate in the body of the ACC NMOSFET **300**. Advantageously, the accumulated charge can be removed via the ACS terminal **408** by connecting the ACS terminal **408** to the control circuit **412** as shown. In order to ensure that the accumulated charge is conveyed from the body of the ACC NMOSFET **300**, the ACS bias voltage V_{ACS} that is applied to the ACS terminal **408** should be equal to or more negative than the gate voltage and more negative than the lesser of Vs and Vd. Because the accumulated charge **120** is conveyed to the bias voltage V_{ACS} applied to the ACS terminal **408** by the control circuit **412**, the accumulated charge does not remain trapped under the gate oxide due to attraction to the gate bias voltage Vg.

In other embodiments, Vs and Vd may comprise bias voltages that are other than zero. According to these examples, Vg must be sufficiently negative to both Vs and Vd in order for Vg to be sufficiently negative to V_{th}, in order to bias the NMOSFET **300** in the off-state. This allows the accumulation of accumulated charge under the gate oxide. For this example, the ACS bias voltage V_{ACS} may be selected to be equal to or more negative than the lesser of Vs and Vd by connecting the ACS terminal **408** to the control circuit **412** to provide selected ACS bias voltages, thereby conveying the accumulated charge from the ACC NMOSFET **300**.

In other embodiments, if the ACC NMOSFET **300** of FIG. **4**D comprises a depletion mode device, V_{th} is, by definition, less than zero. For Vs and Vd both at zero volts, when a gate bias Vg sufficiently negative to V_{th} is applied (for example, Vg more negative than approximately −1 V relative to V_{th}), holes may accumulate under the gate oxide. For this example, the ACS bias voltage V_{ACS} that is applied to the ACS terminal **408** may also be selected to be equal to or more negative than the lesser of Vs and Vd by connecting the ACS terminal **408** to the control circuit **412** and thereby provide the desired ACS bias voltages V_{ACS} that are necessary to remove the accumulated charge from the ACC NMOSFET **300**.

As described above, in one embodiment, instead of having the control circuit **412** provide a bias to the ACS terminal **408** as shown in FIG. **4**D, the ACS terminal **408** can be driven by a separate bias source circuit, as shown, for example, in the embodiment of FIG. **4**E. In one exemplary circuit implementation, as exemplified in the circuit of FIG. **4**E, in an RF switch circuit, the separate V_{ACS} source has a high output impedance element **403** which ensures that the RF voltage is divided across the ACC NMOSFET **300**, and which further ensures that the voltage applied to the ACS terminal **408** has Vds/2 applied thereon, similar to the voltage Vgs that is applied to the gate terminal **402**. In one exemplary embodiment, an inverter **405** is configured in series with the high output impedance element **403** and supplied by GND and $-V_{DD}$. In one exemplary embodiment, $-V_{DD}$ is readily derived from a convenient positive voltage supply. It could, however, comprise an even more negative voltage for improved linearity (i.e., it can be independent of the gate voltage).

In another embodiment, the circuit shown in FIG. **4**C can be modified to include a clamping circuit configured in series with an ACS terminal **408**. Such an exemplary embodiment is shown in FIG. **4**F. Under certain operating conditions, current that flows out of the ACC NMOSFET **300**, conveying the accumulated charge from the body of the ACC NMOSFET **300**, via the ACS terminal **408** is sufficiently high such that it causes problems in the biasing circuitry (i.e., under some conditions the ACS current is so high that the biasing circuitry cannot adequately sink the current flowing out of the body of the ACC NMOSFET **300**). As shown in the circuit of FIG. **4**F, one exemplary embodiment solves this problem by interrupting the flow of ACS current out of the body of the ACC NMOSFET **300**, and thereby returning the ACC NMOSFET **300** to a floating body condition.

In one exemplary circuit, as shown in FIG. **4**F, a depletion-mode FET **421** is configured in series between the ACS terminal **408** and a diode **410**. In this exemplary circuit, the depletion-mode FET **421** includes a gate terminal that is electrically connected to the FET's source terminal. In this configuration, the depletion-mode FET **421** functions to clip or limit the current that flows from the ACS terminal **408** when the ACC MOSFET operates in the accumulated charge regime. More specifically, the depletion-mode FET **421** enters saturation upon reaching a predefined threshold. The current leaving the body of the ACC MOSFET is thereby limited by the saturation current of the FET **421**. In some embodiments, the predefined saturation threshold may optionally be adjusted to change the point at which clamping occurs, such as by selecting a higher threshold voltage, which results in a lower maximum current and earlier clamping.

In some embodiments, such as for example in an RF switch circuit, the gate terminal **402** and the ACS terminal **408** follow Vds at half the rate (Vds/2) of Vds. At high Vds excursions, Vgs may approach the threshold voltage V_{th}, resulting in increased Ids leakage current. In some cases, such a leakage current exits the ACS terminal **408** and can overwhelm associated circuitry (e.g., a negative voltage generator). Hence, the circuit shown in FIG. **4**F solves or otherwise mitigates these problems. More specifically, by coupling the FET **421** in series between the ACS terminal **408** and the diode **410**, the current that exits the ACS terminal **408** is limited to the saturation current of the FET **421**.

In yet another exemplary embodiment, the simplified circuit shown in FIG. **4**C can be modified to include an AC shorting capacitor placed in parallel with the diode **410**. The simplified circuit of FIG. **4**G can be used to compensate for certain undesirable nonlinearities present in a full circuit application. In some embodiments, due to parasitics present in the MOSFET layout, nonlinearity characteristics existing in the diode **410** of FIG. **4**C may introduce undesirable nonlinearities in a full circuit implementation. As the diode is in place to provide DC bias conditions and is not intended to have any AC signals across it, it may be desirable in some

embodiments to take steps to mitigate the effects of any AC signal present across the diode **410**.

As shown in the simplified circuit of FIG. **4**G, the circuit of FIG. **4**C has been modified to include an AC shorting capacitor **423** wherein the AC shorting capacitor **423** is configured in parallel across the diode **410**. The AC shorting capacitor **423** is placed in parallel with the diode **410** to ensure that nonlinearities of the diode **410** are not excited by an AC signal. In some exemplary circuits, such as in an RF switch, the AC shorting capacitor **423** does not impact the higher level full circuit, as the gate terminal **402** and the ACS terminal **408** typically have the same AC signal applied (i.e., AC equipotential).

In some circuit embodiments, body nodes of a multi-finger FET implementation may be connected to one another (using, for example, metal or silicon), overlapping the source fingers. On another side of the FET implementation, gate nodes may be are connected to one another (using, for example, metal or silicon) overlapping the drain fingers. As a result of this FET implementation, additional capacitance may result between the source and body (S-B), and further additional capacitance may result between the drain and gate (D-G). These additional capacitances may degrade the symmetry of the intrinsic device. Under AC excitation, this results in the gate terminal following the drain terminal more closely, and the body terminal following the source terminal more closely, which effectively creates an AC signal across the diode **410**, which can excite nonlinearities of the diode **410** as described above. Using the exemplary embodiment shown in FIG. **4**G, parasitic nonlinear excitation due to the overlapping fingers is mitigated.

Improved C_{off} Performance Characteristics of ACC MOSFETs Made in Accordance with the Present Disclosed Method and Apparatus

FIG. **4**H is a plot **460** of the off-state capacitance (C_{off}) versus an applied drain-to-source voltage of an SOI MOSFET when an AC signal is applied to the MOSFET (the plot **460** is relevant to an exemplary 1 mm wide MOSFET, though similar plots result using wider and narrower devices). In one embodiment, a gate voltage equals −2.5 Volts+Vd/2, and Vs equals 0. A first plot **462** shows the off-state capacitance C_{off} of a typical prior art NMOSFET operating within the accumulated charge regime and thereby having an accumulated charge as described above with reference to FIG. **1**. As shown in FIG. **4**H, the off-state capacitance C_{off} shown in plot **462** of the prior art FET is voltage-dependent (i.e., it is nonlinear) and peaks when Vd=0 Volts. A second plot **464** illustrates the off-state capacitance C_{off} of an improved ACC SOI MOSFET made in accordance with the present teachings, wherein the accumulated charge is conveyed from the ACC MOSFET, thereby reducing, controlling and/or eliminating the accumulated charge from the ACC MOSFET body. As shown in FIG. **4**H, the off-state capacitance C_{off} shown in plot **464** of the ACC SOI MOSFET is not voltage-dependent (i.e., it is linear).

As described above with reference to FIG. **2**A, by controlling, reducing or eliminating the accumulated charge, the impedance **212** of the NMOSFET body **312** (FIG. **3**C, and shown as the MOSFET body **114** in the electrical model of FIG. **2**A) is increased to a very large value. This increase in the impedance **212** of the MOSFET body reduces the contribution to C_{off} caused by the impedance of the junctions **218** and **220** (FIG. **2**A), thereby reducing the overall magnitude of C_{off} and the nonlinear effects associated with the impedances of the junctions **218** and **220**. Plot **464** illustrates how the present teachings advantageously reduce both the nonlinearity and overall magnitude of the off-state capacitance C_{off} of the MOSFET. The reduced nonlinearity and magnitude of the off-state capacitance C_{off} improves the performance of circuits using MOSFETs operating in an accumulated charge regime, such as RF switching circuits. Exemplary RF switching circuits implemented with the ACC MOSFETs described above with reference to FIGS. **4**A-**4**G are now described with reference to FIGS. **5**A-**5**D.

Exemplary Improved Performance RF Switch Implementations Using ACC SOI MOSFETs in Accordance with the Present Teachings

FIG. **5**A shows a schematic diagram of a single pole, single throw (SPST) RF switch circuit **500** in accordance with prior art. The RF switch circuit **500** is one example of a general class of well-known RF switch circuits. Similar RF switch circuits are described in the following co-pending and commonly assigned U.S. Applications and Patent: Provisional Application No. 60/651,736, filed Feb. 9, 2005, entitled "UNPOWERED SWITCH AND BLEEDER CIRCUIT;" application Ser. No. 10/922,135, filed Aug. 18, 2004, pending, which is a continuation application of application Ser. No. 10/267,531, filed Oct. 8, 2002, which issued Oct. 12, 2004 as U.S. Pat. No. 6,804,502, entitled "SWITCH CIRCUIT AND METHOD OF SWITCHING RADIO FREQUENCY SIGNALS". Application Ser. No. 10/267,531, filed Oct. 8, 2002, which issued Oct. 12, 2004 as U.S. Pat. No. 6,804,502 claims the benefit of U.S. Provisional Application No. 60/328,353, filed Oct. 10, 2001. All of the above-cited applications and issued patent set forth above are hereby incorporated by reference herein as if set forth in full for their teachings on RF switch circuits including SOI MOSFET switch circuits.

Referring again to FIG. **5**A, a switching SOI NMOSFET **506** is adapted to receive an RF input signal "RFin" at an input terminal **502**. The switching SOI MOSFET **506** is electrically coupled to selectively couple the RFin input signal to an output terminal **504** (i.e., thereby convey an RF output signal Rfout at the output terminal **504**). In the exemplary embodiment, the switching SOI NMOSFET **506** is controlled by a first control signal **C1** that is conveyed by a control line **512** through a gate resistor **510** (optionally included for suppression of parasitic RF coupling). The control line **512** is electrically coupled to a control circuit **520**, which generates the first control signal **C1**.

Referring again to FIG. **5**A, a shunting SOI NMOSFET **508** is adapted to receive the RF input signal RFin at its drain terminal, and to selectively shunt the input signal RFin to ground via an optional load resistor **518**. The shunting SOI NMOSFET **508** is controlled by a second control signal **C1***x* which is conveyed by a control line **516** through a gate resistor **514** (optionally included for suppression of parasitic RF coupling and for purposes of voltage division). The control line **516** is electrically coupled to the control circuit **520**, which generates the second control signal **C1***x*.

The terms "switching" and "shunting", as pertains to the transistors shown in FIG. **5**A and also described below with reference to the RF switch circuits of FIGS. **5**B-**5**D, **6**, **8**, and **9**, are used interchangeably herein with the terms "switch" and "shunt", respectively. For example, the switching transistor **506** (and all of its analogous switching transistors described below in FIGS. **5**B-**5**D, **6**, **8**, and **9**) is also referred to herein as the "switch" transistor. Similarly, the shunting transistor **508** (and all of its analogous shunting transistors described below in FIGS. **5**B-**5**D, **6**, **8**, and **9**) is also referred to herein as the "shunt" transistor. The terms "switch" and "switching" (and similarly the terms "shunt" and "shunting"), when used to describe the RF switch circuit transistors, are used interchangeably herein. Further, as described below

in more detail with reference to FIG. **6**, those skilled in the RF switching design and fabrication arts shall recognize that although the switch and shunt transistors are shown in FIGS. **5**A-**5**D and FIG. **9** as comprising a single MOSFET, it shall be understood that they may comprise transistor groupings comprising one or more MOSFET transistors.

It will also be appreciated by those skilled in RF switch circuits that all of the exemplary switch circuits may be used "bi-directionally," wherein the previously described input ports function as output ports, and vice versa. That is, although an exemplary RF switch may be described herein as having one or more input ports (or nodes) and one or more output ports (or nodes), this description is for convenience only, and it will be understood that output ports may, in some applications, be used to input signals, and input ports may, in some applications, be used to output signals. The RF switch circuits described with reference to FIGS. **2**B, **4**E, **5**A-**5**D, **6**, **8** and **9** are described herein as having "input" and "output" ports (or "nodes") that input and output RF signals, respectively. For example, as described below in more detail with reference to FIG. **9**, RF input node **905** and RF input node **907** are described below as inputting RF signals RF**1** and RF**2** respectively. RFC common port **903** is described below as providing an RF common output signal. Those skilled in the RF switch circuit design arts shall recognize that the RF switch is bidirectional, and that the previously described input ports function perfectly well as output ports, and vice versa. In the example of the RF switch of FIG. **9**, the RFC common port can be used to input an RF signal which is selectively output by the RF nodes **905** and **907**.

Referring again to FIG. **5**A, the first and second control signals, C**1** and C**1***x*, respectively, are generated so that the switching SOI NMOSFET **506** operates in an on-state when the shunting SOI NMOSFET **508** operates in an off-state, and vice versa. These control signals provide the gate bias voltages Vg to the gate terminals of the NMOSFETs **506** and **508**. When either of the NMOSFETs **506** or **508** is biased to select the transistor off-state, the respective Vg must comprise a sufficiently large negative voltage so that the respective NMOSFET does not enter, or approach, an on-state due to the time varying applied voltages of the RF input signal RFin. The maximum power of the RF input signal RFin is thereby limited by the maximum magnitude of the gate bias voltage Vg (or, more generally, the gate-to-source operating voltage, Vgs) that the SOI NMOSFETs **506** and **508** can reliably sustain. For RF switching circuits such as those exemplified herein, the magnitude of Vgs(max)=|Vg|+|Vds(max)/2|, where Vds=Vd−Vs, and Vds(max) comprises the maximum Vds due to the high-power input signal voltage levels associated with the RF input signal RFin.

Exemplary bias voltages for the switching and shunting SOI NMOSFETs **506** and **508**, respectively, may include the following: with V_{th} approximately zero volts, Vg, for the on-state, of +2.5 V, and Vg, for the off-state, of −2.5 V. For these bias voltages, the SOI NMOSFETs may eventually operate in an accumulated charge regime when placed into their off-states. In particular, and as described above with reference to FIG. **2**B, when the switching NMOSFET **506** is in the on-state, and the shunting NMOSFET **508** is biased in the off-state, the output signal RFout may become distorted by the nonlinear behavior of the off capacitance C_{off} of the shunting NMOSFET **508** caused by the accumulated charge. Advantageously, the improved ACC MOSFETs made in accordance with the present teachings can be used to improve circuit performance, especially as it is adversely affected by the accumulated charge.

FIG. **5**B is a schematic of an improved RF circuit **501** adapted for higher performance using the present accumulated charge reduction and control techniques. The switch circuit **501** differs from the prior art circuit **500** (FIG. **5**A) in that the shunting NMOSFET **508** is replaced by a shunting ACC NMOSFET **528** made in accordance with the present teachings. The shunting ACC NMOSFET **528** is analogous to the ACC NMOSFET described above with reference to FIGS. **4**A and **4**B. Similarly, the gate, source, drain and ACC terminals of the shunting ACC NMOSFET **528** are analogous to the respective terminals of the ACC NMOSFET **300**. With the exception of the improved switch performance afforded by the improved shunting ACC NMOSFET **528**, the operation of the RF switch circuit **501** is very similar to the operation of the RF switch circuit **500** described above with reference to FIG. **5**A.

Exemplary bias voltages for the switching NMOSFET **526** and the shunting ACC NMOSFET **528** may include: with V_{th} approximately zero, Vg, for the on-state, of +2.5 V, and Vg, for the off-state, of −2.5 V. For these bias voltages, the SOI NMOSFETs may operate in an accumulated charge regime when placed into the off-state. However, when the switching NMOSFET **526** is in the on-state and the shunting ACC NMOSFET **528** is in the off-state, the output signal RFout at the output terminal **505** will not be distorted by nonlinear behavior of the off-state capacitance C_{off} of the improved shunting ACC NMOSFET **528** due to the accumulated charge. When the shunting ACC NMOSFET **528** operates in the accumulated charge regime, the accumulated charge is removed via the ACS terminal **508'**. More specifically, because the gate terminal **502'** of the shunting ACC NMOSFET **528** is connected to the ACS terminal **508'**, the accumulated charge is removed or otherwise controlled as described above in reference to the simplified circuit of FIG. **4**B. The control of the accumulated charge improves performance of the switch **501** by improving the linearity of the off transistor, shunting ACC NMOSFET **528**, and thereby reducing the harmonic and intermodulation distortion of the RF output signal Rfout generated at the output terminal **505**.

FIG. **5**C is a schematic of another embodiment of an improved RF switch circuit **502** adapted for higher performance using the accumulated charge control techniques of the present disclosure. The switch circuit **502** differs from the prior art circuit **500** (FIG. **5**A) in that the NMOSFET **508** is replaced by an ACC NMOSFET **528** made in accordance with the present teachings. The ACC NMOSFET **528** is analogous to the ACC NMOSFET **300** described above with reference to FIGS. **4**A and **4**C. Similarly, the gate, source, drain and ACC terminals of the ACC NMOSFET **528** are analogous to the respective terminals of the ACC NMOSFETs **300** described above with reference to FIGS. **4**A and **4**C. With the exception of the improved switch performance afforded by the improved ACC NMOSFET **528**, the operation of the switch circuit **502** is very similar to the operations of the switch circuits **500** and **501** described above with reference to FIGS. **5**A and **5**B, respectively.

Exemplary bias voltages for the NMOSFET **526** and the ACC NMOSFET **528** may include the following: with V_{th} approximately zero volts, Vg, for the on-state, of +2.5 V, and Vg, for the off-state, of −2.5 V. For these bias voltages, the SOI NMOSFETs **526**, **528** may operate in an accumulated charge regime when placed into an off-state. However, when the NMOSFET **526** is in the on-state and the ACC NMOSFET **528** is in the off-state, the output signal RFout will not be distorted by nonlinear behavior of the off-state capacitance C_{off} of the ACC NMOSFET **528** due to the accumulated charge. Because the gate terminal **502'** of the ACC NMOS-

FET **528** is connected to the ACS terminal **508'** via a diode **509**, the accumulated charge is entirely removed, reduced or otherwise controlled, as described above with reference to FIG. **4**C. Similar to the improved switch **501** described above with reference to FIG. **5**B, control of the accumulated charge improves performance of the switch **502** by improving the linearity of the off transistor, **528**, and thereby reducing the harmonic and intermodulation distortion of the RF output signal Rfout output of the RF output terminal **505**. Connection of the diode **509** as shown may be desired in some embodiments for suppression of positive current flow into the ACC NMOSFET **528** when it is biased into an on-state, as described above with reference to FIG. **4**C.

FIG. **5**D is a schematic of another embodiment of an improved RF switch circuit **503** adapted for higher performance using the present accumulated charge control techniques. The switch circuit **503** differs from the prior art circuit **500** (FIG. **5**A) in that the NMOSFET **508** of FIG. **5**A is replaced by an ACC NMOSFET **528** made in accordance with the present teachings. The ACC NMOSFET **528** is analogous to the ACC NMOSFET described above with reference to FIGS. **4**A and **4**D. With the exception of the improved switch performance afforded by the improved ACC NMOSFET **528**, the operation of the switch circuit **503** is very similar to the operations of the switch circuits **500**, **501** and **502** described above with reference to FIGS. **5**A-**5**C, respectively.

Exemplary bias voltages for the NMOSFET **526** and the ACC NMOSFET **528** may include the following: with V_{th} approximately zero volts, Vg, for the on-state, of +2.5 V, and Vg, for the off-state, of −2.5 V. For these bias voltages, the SOI NMOSFETs **526**, **528** may operate in an accumulated charge regime when placed into the off-state. However, when the NMOSFET **526** is in the on-state and the ACC NMOSFET **528** is in the off-state, the output signal RFout produced at the output terminal **505** will not be distorted by the nonlinear behavior of the off-state capacitance C_{off} of the ACC NMOSFET **528** due to the accumulated charge. When the NMOSFET **528** operates in the accumulated charge regime, the accumulated charge is removed via the ACS terminal **508'**. More specifically, because the ACS terminal **508'** of the ACC NMOSFET **528** is electrically coupled to the control circuit **520** via the control line **517** (i.e., controlled by the control signal "**C2**" as shown), the accumulated charge can be eliminated, reduced or otherwise controlled by applying selected bias voltages to the ACS terminal **508'** as described above with reference to FIG. **4**D. Those skilled in the arts of electronic circuit design shall understand that a wide variety of bias voltage signals can be applied to the ACS terminal for the purpose of reducing or otherwise controlling the accumulated charge. The specific bias voltages may be adapted for use in a particular application. The control of the accumulated charge improves performance of the switch **503** by improving the linearity of the off-state transistor, **528**, and thereby reducing the harmonic and intermodulation distortion of the RF output signal Rfout generated at the output terminal **505**.

In the circuits described above with respect to FIGS. **5**B-**5**D, the switching SOI MOSFETs **526** are shown and described as implemented using SOI MOSFETs of the prior art (i.e., they do not comprise ACC MOSFETs and therefore do not have an ACS terminal). Those skilled in the electronic device design arts shall understand and appreciate that in other embodiments of the disclosed method and apparatus, the prior art switching SOI MOSFETs **526** may be replaced, as desired or required, by ACC SOI MOSFETs made in accordance with the present disclosure. For example, in some embodiments of RF switches implemented using the ACC MOSFET of the present teachings, the RF switch comprises a single-pole double-throw RF switch. In this embodiment, the switching SOI MOSFETs (e.g., analogous to the switching SOI MOSFETs **526** described above with reference to FIGS. **5**B-**5**D) may comprise ACC SOI MOSFETs. Such an implementation prevents nonlinear behavior of the off-state switching SOI MOSFETs (which is turned off when it is not selected as an input "pole") from detrimentally affecting the output of the RF signal as switched through the selected "pole". Implementation of the RF switches using switching ACC MOSFETs reduces the magnitude, drift, and voltage dependency of the off capacitance C_{off} of the switching transistors. Consequently, and as described above in more detail, the switch performance characteristics, such as its isolation, insertion loss and drift characteristics, are also improved. This implementation is described in more detail below with reference to the RF switch circuit shown in FIG. **9**. Many other examples will be apparent to those skilled in the arts of electronic circuits.

For example, as set forth above, although the exemplary RF switches have been described as being implemented using ACC SOI NMOSFET devices, they can also be implemented using ACC SOI PMOSFET devices. Further, although single-pole single-throw, and single-pole double-throw RF switches have been described above as examples of RF switches implemented in accordance with the present teachings, the present application encompasses any variation of single-pole multi-throw, multi-pole single-throw, and multi-pole multi-throw RF switch configurations. Those skilled in the RF switch design and fabrication arts shall recognize and appreciate that the present teachings can be used in implementing any convenient RF switch configuration design.

Exemplary RF Switch Implementation Using Stacked Transistors

In the exemplary embodiments of RF switch circuits described above, the switch circuits are implemented using a single SOI NMOSFET (e.g., the single SOI NMOSFET **506** of FIG. **5**A, and the single SOI NMOSFET **526** of FIGS. **5**B-**5**D) that selectively couples or blocks (i.e., electrically opens the circuit connection) the RF input signal to the RF output. Similarly, in the exemplary embodiments described above with reference to FIGS. **5**A-**5**D, a single SOI NMOSFET (e.g., the single SOI NMOSFET **508** of FIG. **5**A, and ACC SOI NMOSFET **528** of FIGS. **5**B-**5**D) is used to shunt (FET in the on-state) or block (FET in the off-state) the RF input signal to ground. Commonly assigned U.S. Pat. No. 6,804,502, entitled "SWITCH CIRCUIT AND METHOD OF SWITCHING RADIO FREQUENCY SIGNALS", issued Oct. 12, 2004, describes RF switch circuits using SOI NMOSFETs implemented with stacked transistor groupings that selectively couple and block RF signals.

One example of how stacked NMOSFETs may be implemented in accordance with the teachings of the present disclosure is illustrated in FIG. **6**. An RF switch circuit **600** is analogous to the RF switch circuit **503** of FIG. **5**D, wherein the single SOI NMOSFET **526** is replaced by a stack of SOI NMOSFETs **602**, **604** and **606**. Similarly, the single ACC SOI NMOSFET **528** is replaced by a stack of ACC SOI NMOSFETs **620**, **622** and **624**. The control signal C2 is provided to the ACS terminals of the ACC SOI NMOSFETs **620**, **622** and **624** via optional resistors **626**, **628**, and **630**, respectively. The resistors **626**, **628**, and **630** may optionally be included in order to suppress parasitic RF signals between the stacked ACC SOI NMOSFETs **620**, **622**, and **624**, respectively. The RF switch circuit **600** operates analogously to the operation of the RF switch circuit **503** described above with reference to FIG. **5**D.

Three stacked ACC SOI NMOSFETs are shown in each ACC NMOSFET stack in the exemplary stacked RF switch circuit **600** of FIG. **6**. A plurality of three ACC NMOSFETs is shown for illustrative purposes only, however, those skilled in the integrated circuit design arts will understand that an arbitrary plurality may be employed according to particular circuit requirements such as power handling performance, switching speed, etc. A smaller or larger plurality of stacked ACC NMOSFETs may be included in a stack to achieve a desired operating performance.

Other stacked RF switch circuits, adapted for accumulated charge control, analogous to the circuits described above with reference to FIGS. **5**B-**5**D, may also be employed. Implementations of such circuits shall be obvious from the teachings above to those skilled in the electronic device design arts, and therefore are not described further herein. Moreover, is shall be obvious to those skilled in the electronic device design arts that, although a symmetrically stacked (i.e., having an equal number of shunting and switching transistors) RF switch is shown in the stacked RF switch of FIG. **6**, the present inventive ACC method and apparatus is not so limited. The present teachings can be applied in implementing both symmetrically and asymmetrically stacked (having an unequal number of shunting and switching transistors) RF switches. The designer will readily understand how to use the ACC MOSFETs of the present disclosure in implementing asymmetrical, as well as symmetrical, RF switch circuits.

Exemplary Method of Operation

FIG. **7** illustrates an exemplary method **700** of improving the linearity of an SOI MOSFET having an accumulated charge sink (ACS) in accordance with the present disclosure. The method **700** begins at a STEP **702**, whereat an ACC SOI MOSFET having an ACS terminal is configured to operate in a circuit. The ACS terminal may be operatively coupled to the gate of the SOI MOSFET (as described above with reference to FIGS. **4**B, **4**C, **5**B and **5**C), or to a control circuit (as described above with reference to FIGS. **4**D and **5**D). In other embodiments, the ACS terminal may be operatively coupled to any convenient accumulated charge sinking mechanism, circuit, or device as is convenient to the circuit or system designer. The method then proceeds to a step **704**.

At the STEP **704**, the ACC SOI MOSFET is controlled, at least part of the time, so that it operates in an accumulated charge regime. In most embodiments, as described above, the ACC MOSFET is operated in the accumulated charge regime by applying bias voltages that place the FET in an off-state condition. In one exemplary embodiment, the ACC SOI MOSFET comprises an ACC SOI NMOSFET that is configured as part of a shunting circuit of an RF switch. According to this exemplary embodiment, the SOI NMOSFET may be operated in an accumulated charge regime after the shunting circuit is placed into an off-state by applying a negative bias voltage to the gate terminal of the ACC NMOSFET.

The method then proceeds to a STEP **706**, whereat the accumulated charge that has accumulated in the channel region of the ACC MOSFET is removed or otherwise controlled via the ACS terminal. In this embodiment, the accumulated charge is conveyed to another circuit terminal and is thereby reduced or otherwise controlled. One such exemplary circuit terminal that can be used to convey the accumulated charge from the MOSFET body comprises a gate terminal of the ACC MOSFET (see, e.g., the description above with reference to FIGS. **4**B, **4**C, **5**B and **5**C). Another exemplary circuit terminal that can be used to remove or otherwise control the accumulated charge comprises the terminal of a control circuit (see, e.g., FIGS. **4**D and **5**D). As described in more detail above, removing or otherwise controlling the accumulated charge in the ACC MOSFET body improves the linearity of the off-state ACC MOSFET, which reduces the harmonic distortion and IMD of signals affected by the ACC MOSFET, and which, in turn, improves circuit and system performance. In RF switch circuits, improvements (in both linearity and magnitude) are made to the off capacitance of shunting ACC MOSFET devices, which, in turn, improves the performance of the RF switch circuits. In addition to other switch performance characteristics, the harmonic and intermodulation distortions of the RF switch are reduced using the ACC method and apparatus of the present teachings.

FIGS. **8** and **9** show schematics of additional exemplary embodiments of RF switching circuits made in accordance with the disclosed method and apparatus for use in improving linearity of MOSFETs having an ACS. As described in more detail below with reference to FIGS. **8** and **9**, in some exemplary embodiments of RF switch circuits made in accordance with the present disclosure, it may be desirable to include drain-to-source resistors, Rds, and thereby improve some switch performance characteristics when the switch is used in a particular application. These exemplary RF switch circuits are now described in more detail.

Exemplary RF Switch Implementations Using Stacked Transistors having Source to Drain Resistors

FIG. **8** shows one exemplary embodiment of an RF switch circuit **800** made in accordance with the present disclosure. As shown in FIG. **8**, some embodiments of RF switches made in accordance with the present disclosure may include drain-to-source (R_{ds}) resistors electrically connected to the respective sources and drains of the ACC MOSFETs. For example, the exemplary switch **800** of FIG. **8** includes drain-to-source R_{ds} resistors **802**, **804**, and **806** electrically connected to the respective sources and drains of the shunting ACC SOI NMOSFETs **620**, **622**, and **624**, respectively. Motivation for use of the drain-to-source R_{ds} resistors is now described.

As shall be appreciated by skilled persons from the present teachings, removal of the accumulated charge via the ACS terminal causes current to flow from the body of the ACC SOI MOSFET. For example, when a hole current flows from the body of an ACC SOI MOSFET via the ACS, an equal electron current flows to the FET source and/or drain. For some circuits (e.g., the RF switch circuit of FIG. **8**), the sources and/or drains of the ACC SOI NMOSFETs are connected to other SOI NMOSFETs. Because off-state SOI NMOSFETs have a very high impedance (e.g., in the range of 1 Gohm for a 1 mm wide SOI NMOSFET), even a very small drain-to-source current (e.g., in the range of 1 nA) can result in an unacceptably large drain-to-source voltage Vds across the ACC SOI NMOSFET in satisfaction of Kirchhoffs well known current and voltage laws. In some embodiments, such as that shown in the RF switch circuits of FIGS. **8** and **9**, such resultant very large drain-to-source voltages Vds undesirably impacts reliability and linearity of the ACC SOI NMOSFET. The drain-to-source resistors R_{ds} provide a path between the ACC FET drain and source whereby currents associated with controlling the accumulated charge may be conducted away from the sources and drains of ACC SOI NMOSFETs when implemented in series with high impedance elements such as other ACC SOI NMOSFETs.

Exemplary operating voltages for the NMOSFETs **602**-**606** of FIG. **8**, and the ACC NMOSFETs **620**-**624**, may include the following: V_{th} approximately zero volts, Vg, for the on-state, of +2.5 V, and Vg, for the off-state, of −2.5 V. In an exemplary embodiment, the ACC SOI NMOSFET **622** of FIG. **8** may have a width of 1 mm, and an electron-hole pair generation rate for accumulated charge producing a current of 10 pA/μm for operation in the accumulated charge regime.

For the electron current supplied equally by the source and drain, and an impedance of the ACC SOI NMOSFETs **620** and **622** on the order of 1 Gohm, then an unacceptable bias of −5 V would result on the source and drain of the ACC SOI NMOSFET **622** without the presence of R_{ds} resistors **802** and **806**. This bias voltage would also be applied to the interior nodes of the ACC SOI NMOSFETs **620** and **624**.

Even currents smaller than the exemplary currents may produce adverse affects on the operation of the RF switching circuit **800** by reducing Vgs and/or Vgd of the ACC SOI MOSFETs **620-624** in the off-state, thereby reducing the power handling capability and reliability of the circuit by increasing leakage (e.g., when either Vgs or Vgd approaches V_{th}), by increasing hot-carrier damage caused by excess leakage, etc. Linearity of the MOSFETs is also degraded by reducing Vgs and/or Vgd when either value approaches V_{th}.

Exemplary values for the R_{ds} resistors **802** to **806** may be selected in some embodiments by selecting a value approximately equal to the resistance of the gate resistors **632-636** divided by the number of ACC SOI NMOSFETs in the stack (in the exemplary embodiment, there are three ACC FETs in the stack). More generally, the value of the R_{ds} resistors may be equal to the gate resistor value divided by the number of ACC SOI NMOSFETs in the stack. In one example, a stack of eight ACC SOI NMOSFETs may have gate resistors of 80 kohm and R_{ds} resistors of 10 kohm.

In some embodiments, the R_{ds} resistors may be selected so that they do not adversely affect switch performance characteristics, such as, for example, the insertion loss of the switch **800** due to the off-state ACC SOI NMOSFETs. For example, for a net shunt resistance greater than **10** kohm, the insertion loss is increased by less than 0.02 dB.

In other embodiments, the R_{ds} resistors may be implemented in circuits comprising a single ACC SOI MOSFET (as contrasted with the stacked shunting configuration exemplified in FIG. **8** by the shunting ACC FETs **620**, **622** and **624**). For example, such circuits may be desirable if there are other high-impedance elements configured in series with an ACC SOI MOSFET that may cause a significant bias voltage to be applied to the source or drain as a result of the current flow created when removing or otherwise controlling accumulated charge. One exemplary embodiment of such a circuit is shown in FIG. **9**.

FIG. **9** shows an exemplary single-pole double-throw (SPDT) RF switch circuit **900** made in accordance with the present teachings. As shown in FIG. **9**, a DC blocking capacitor **904** is connected to a first RF input node **905** that receives a first RF input signal RF**1**. Similarly, a DC blocking capacitor **906** is connected to a second RF input node **907** that receives a second RF input signal RF**2**. Further, a DC blocking capacitor **902** is electrically connected to an RF common output node **903** that provides an RF common output signal (RFC) selectively conveyed to the node RFC **903** by the switch circuit **900** from either the first RF input node **905** or the second RF input node **907** (i.e., RFC either outputs RF**1** or RF**2**, depending upon the operation of the switch as controlled by the control signals C**1** and C**1***x* described below in more detail).

A first control signal C**1** is provided to control the operating states of the ACC SOI NMOSFETs **526** and **528'** (i.e., C**1** selectively operates the FETs in the on-state or the off-state). Similarly, a second control signal C**1***x* is provided to control the operating states of the ACC SOI NMOSFETs **528** and **526'**. As is well known, and as described for example in the above incorporated commonly assigned U.S. Pat. No. 6,804,502, the control signals C**1** and C**1***x* are generated so that the ACC SOI NMOSFETs **526** and **528'** are in an on-state when the ACC SOI NMOSFETs **528** and **526'** are in an off-state, and vice versa. This configuration allows the RF switch circuit **900** to selectively convey either the signal RF**1** or RF**2** to the RF common output node **903**.

A first ACS control signal C**2** is configured to control the operation of the ACS terminals of the SOI NMOSFETs **526** and **528'**. A second ACS control signal C**2***x* is configured to control the ACS terminals of the ACC SOI NMOSFETs **528** and **526'**. The first and second ACS control signals, C**2** and C**2***x*, respectively, are selected so that the ACSs of the associated and respective NMOSFETs are appropriately biased in order to eliminate, reduce, or otherwise control their accumulated charge when the ACC SOI NMOSFETs operate in an accumulated charge regime.

As shown in the RF switch circuit **900** of FIG. **9**, in some embodiments, an Rd, resistor **908** is electrically connected between the source and drain of the switching ACC NMOSFET **526**. Similarly, in some embodiments, an R_{ds} resistor **910** is electrically connected between the source and drain of the switching ACC NMOSFET **526'**. According to this example, the circuit **900** is operated so that either the shunting ACC NMOSFET **528** or the shunting ACC NMOSFET **528'** operate in an on-state at any time (i.e., at least one of the input signals RF **1** at the node **905** or RF**2** at the node **907** is always conveyed to the RFC node **903**), thereby providing a low-impedance path to ground for the node **905** or **907**, respectively. Consequently, either the Rd, resistor **908** or the R_{ds} resistor **910** provides a low-impedance path to ground from the RF common node **903**, thereby preventing voltage bias problems caused as a result of ACC current flow into the nodes **903**, **905** and **907** that might otherwise be caused when using the DC blocking capacitors **902**, **904** and **906**.

Additional Exemplary Benefits Afforded by the ACC MOSFETs of the Present Disclosure

As described above, presence of the accumulated charge in the bodies of the SOI MOSFETs can adversely affect the drain-to-source breakdown voltage (BVDSS) performance characteristics of the floating body MOSFETs. This also has the undesirable effect of worsening the linearity of off-state MOSFETs when used in certain circuits such as RF switching circuits. For example, consider the shunting SOI NMOSFET **528** shown in FIG. **9**. Further consider the case wherein the shunting NMOSFET **528** is implemented with a prior art SOI NMOSFET, rather than with the ACC NMOSFET made in accordance with the present teachings. Assume that the RF transmission line uses a 50-ohm system. With small signal inputs, and when the NMOSFET **528** operates in an off-state, the prior art off-state shunting NMOSFET **528** may introduce harmonic distortion and/or intermodulation distortion in the presence of multiple RF signals This will also introduce a noticeable loss of signal power.

When sufficiently large signals are input that cause the NMOSFET **528** to enter a BVDSS regime, some of the RF current is clipped, or redirected through the NMOSFET **528** to ground, resulting in a loss of signal power. This current "clipping" causes compression behavior that can be shown, for instance, in a RF switch "Pout vs. Pin" plot. This is frequently characterized by P1 dB, wherein the insertion loss is increased by 1.0 dB over the small-signal insertion loss. This is an obvious indication of nonlinearity of the switch. In accordance with the present disclosed method and apparatus, removing, reducing or otherwise controlling the accumulated charge increases the BVDSS point. Increases to the BVDSS point of the NMOSFET **528** commensurately increases the large-signal power handling of the switch. As an example, for a switch, doubling the BVDSS voltage of the ACC NMOS-

FET increases the P1 dB point by 6 dB. This is a significant accomplishment as compared with the prior art RF switch designs.

In addition, as described above in more detail, presence of the accumulated charge in SOI MOSFET body adversely impacts the magnitude of C_{off} and also takes time to form when the FET is switched from an on-state to an off-state. In terms of switch performance, the nonlinearity of C_{off} adversely impacts the overall switch linearity performance (as described above), and the magnitude of C_{off} adversely affects the small-signal performance parameters such as insertion loss, insertion phase (or delay), and isolation. By reducing the magnitude of C_{off} using the present disclosed method and apparatus, the switch (implemented with ACC MOSFETs) has reduced insertion loss due to lowered parasitic capacitance, reduced insertion phase (or delay), again due to lowered parasitic capacitance, and increased isolation due to less capacitive feedthrough.

The ACC MOSFET also improves the drift characteristic of SOI MOSFETs as pertains to the drift of the small-signal parameters over a period of time. As the SOI MOSFET takes some time to accumulate the accumulated charge when the switch is off, the C_{off} capacitance is initially fairly small. However, over a period of time while operated in the accumulated charge regime, the off-state capacitance C_{off} increases toward a final value. The time it takes for the NMOSFET to reach a full accumulated charge state depends on the electron-hole pair (EHP) generation mechanism. Typically, this time period is on the order of approximately hundreds of milliseconds for thermal EHP generation at room temperature, for example. During this charge-up time period, the insertion loss and insertion phase increase. Also, during this time period, the isolation decreases. As is well known, these are undesirable phenomena in standard SOI MOSFET devices. These problems are alleviated or otherwise mitigated using the ACC NMOSFETs and related circuits described above.

In addition to the above-described benefits afforded by the disclosed ACC MOSFET method and apparatus, the disclosed techniques also allow the implementation of SOI MOSFETs having improved temperature performance, improved sensitivity to Vdd variations, and improved sensitivity to process variations. Other improvements to the prior art SOI MOSFETs afforded by the present disclosed method and apparatus will be understood and appreciated by those skilled in the electronic device design and manufacturing arts.

Exemplary Fabrication Methods

In one embodiment of the present disclosure, the exemplary RF switches described above may be implemented using a fully insulating substrate semiconductor-on-insulator (SOI) technology. Also, as noted above, in addition to the commonly used silicon-based systems, some embodiments of the present disclosure may be implemented using silicon-germanium (SiGe), wherein the SiGe is used equivalently in place of silicon.

In some exemplary embodiments, the MOSFET transistors of the present disclosure may be implemented using "Ultra-Thin-Silicon (UTSi)" (also referred to herein as "ultrathin silicon-on-sapphire") technology. In accordance with UTSi manufacturing methods, the transistors used to implement the inventive methods disclosed herein are formed in an extremely thin layer of silicon in an insulating sapphire wafer. The fully insulating sapphire substrate enhances the performance characteristics of the inventive RF circuits by reducing the deleterious substrate coupling effects associated with non-insulating and partially insulating substrates. For example, insertion loss improvements may be realized by lowering the transistor on-state resistances and by reducing parasitic substrate conductance and capacitance. In addition, switch isolation is improved using the fully insulating substrates provided by UTSi technology. Owing to the fully insulating nature of silicon-on-sapphire technology, the parasitic capacitance between the nodes of the RF switches is greatly reduced as compared with bulk CMOS and other traditional integrated circuit manufacturing technologies.

Examples of and methods for making silicon-on-sapphire devices that can be implemented in the MOSFETs and circuits described herein, are described in U.S. Pat. No. 5,416,043 ("Minimum charge FET fabricated on an ultrathin silicon on sapphire wafer"); U.S. Pat. No. 5,492,857 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); U.S. Pat. No. 5,572,040 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); U.S. Pat. No. 5,596,205 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); U.S. Pat. No. 5,600,169 ("Minimum charge FET fabricated on an ultrathin silicon on sapphire wafer"); U.S. Pat. No. 5,663,570 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); U.S. Pat. No. 5,861,336 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); U.S. Pat. No. 5,863,823 ("Self-aligned edge control in silicon on insulator"); U.S. Pat. No. 5,883,396 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); U.S. Pat. No. 5,895,957 ("Minimum charge FET fabricated on an ultrathin silicon on sapphire wafer"); U.S. Pat. No. 5,920,233 ("Phase locked loop including a sampling circuit for reducing spurious side bands"); U.S. Pat. No. 5,930,638 ("Method of making a low parasitic resistor on ultrathin silicon on insulator"); U.S. Pat. No. 5,973,363 ("CMOS circuitry with shortened P-channel length on ultrathin silicon on insulator"); U.S. Pat. No. 5,973,382 ("Capacitor on ultrathin semiconductor on insulator"); and U.S. Pat. No. 6,057,555 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"). All of these referenced patents are incorporated herein in their entirety for their teachings on ultrathin silicon-on-sapphire integrated circuit design and fabrication.

Similarly to other bulk and SOI CMOS processes, an SOS enhancement mode NMOSFET, suitable for some embodiments of the present disclosure, may, in some embodiments, be fabricated with a p-type implant into the channel region with n-type source and drain regions, and may have a threshold voltage of approximately +500 mV. The threshold voltage is directly related to the p-type doping level, with higher doping resulting in higher thresholds. Similarly, the SOS enhancement mode PMOSFET may, in some exemplary embodiments, be implemented with an n-type channel region and p-type source and drain regions. Again, the doping level defines the threshold voltage with higher doping resulting in a more negative threshold.

In some exemplary embodiments, an SOS depletion-mode NMOSFET, suitable for some embodiments of the present disclosure, may be fabricated by applying the p-type channel-implant mask to the n-type transistor, resulting in a structure that has n-type channel, source, and drain regions and a negative threshold voltage of approximately −500 mV. Similarly, in some exemplary embodiments, a suitable depletion-mode PMOSFET may be implemented by applying the n-type channel-implant mask to the p-type transistor, resulting in a structure that has p-type channel, source, and drain regions and a positive threshold voltage of approximately +500 mV.

As noted in the background section above, the present ACC MOSFET apparatus can also be implemented using any convenient semiconductor-on-insulator technology, included, but not limited to, silicon-on-insulator, silicon-on-sapphire, and silicon-on-bonded wafer technology. One such silicon-on-bonded wafer technique uses "direct silicon bonded" (DSB) substrates. Direct silicon bond (DSB) substrates are fabricated by bonding and electrically attaching a film of single-crystal silicon of differing crystal orientation onto a base substrate. Such implementations are available from the Silicon Genesis Corporation headquartered in San Jose, Calif. As described at the Silicon Genesis Corporation website (publicly available at "www.sigen.com"), silicon-on-bonded wafer techniques include the so-called NanoCleave™ bonding process which can be performed at room temperature. Using this process, SOI wafers can be formed with materials having substantially different thermal expansion coefficients, such as in the manufacture of Germanium-on-Insulator wafers (GeOI). Exemplary patents describing silicon-on-bonded wafer implementations are as follows: U.S. Pat. No. 7,056,808, issued Jun. 6, 2006 to Henley, et al.; U.S. Pat. No. 6,969,668, issued Nov. 29, 2005 to Kang, et al.; U.S. Pat. No. 6,908,832, issued Jun. 21, 2005 to Farrens et al.; U.S. Pat. No. 6,632,724, issued Oct. 14, 2003 to Henley, et al. and U.S. Pat. No. 6,790,747, issued Sep. 14, 2004 to Henley, et al. All of the above-cited patents are incorporated by reference herein for their teachings on techniques and methods of fabricating silicon devices on bonded wafers.

A reference relating to the fabrication of enhancement-mode and depletion-mode transistors in SOS is "CMOS/SOS/LSI Switching Regulator Control Device," Orndorff, R. and Butcher, D., Solid-State Circuits Conference, Digest of Technical Papers, 1978 IEEE International, Volume XXI, pp. 234-235, February 1978. The "Orndorff" reference is hereby incorporated in its entirety herein for its techniques on the fabrication of enhancement-mode and depletion-mode SOS transistors.

Exemplary Results—Appendix A

Exemplary results that can be obtained using the disclosed method and apparatus for use in improving the linearity of MOSFETs are described in the attached Appendix A, entitled "Exemplary Performance Results of an SP6T Switch Implemented with ACC MOSFETs". The contents of Appendix A are hereby incorporated by reference herein in its entirety. The results shown in detail in Appendix A are now briefly described. As noted in the attached Appendix A, the measured results are provided for a single pole, six throw (SP6T) RF switch. Those skilled in the art of RF switch circuit design shall understand that the results can be extended to any practical RF switch configuration, and therefore are not limited to the exemplary SP6T switch for which results are shown.

Slides 2-7 of Appendix A show harmonic performance versus Input Power for prior art devices and for ACC MOSFET devices made in accordance with the present disclosed method and apparatus. Switch circuits implemented with the ACC MOSFET of the disclosed method and apparatus have a third harmonic response that rises at a 3:1 slope (cube of the input) versus input power on the log scale. Those skilled in the electronic device design arts shall appreciate that no input-power dependent dynamic biasing occurs with the improved RF switch designs made in accordance with the present disclosure. In contrast, prior art floating body FET harmonics disadvantageously do not follow a 3:1 slope. This is disadvantageous for small-signal third-order distortions such as IM3.

As shown in the attached Appendix A, at a GSM maximum input power of +35 dBm, the 3 fo is improved by 14 dB. This is shown in detail in slide number 3 of the attached Appendix A. Improvements in third order harmonic distortion is also applicable to all odd order responses, such as, for example, 5^{th} order responses, 7^{th} order responses, etc.

Similar to 3 fo, the second order response of the improved ACC MOSFET-implemented RF switch follows a 2:1 slope (square of the input) whereas the prior art RF switch does not. This results in improved 2 fo and IM2 performance at low input power, and roughly the same performance at +35 dBm.

Slide numbers 6 and 7 of the attached Appendix A treat the performance under non 50-ohm loads. In this case, the load represents a 5:1 mismatch wherein the load impedance can be of any convenient value that results in a reflection coefficient magnitude of ⅔. In the case of SOI MOSFETs, reflection coefficients that result in higher voltages cause the most severe problems. At 5:1 VSWR, the voltage can be 1.667× higher. Those skilled in the art may view this similarly by sweeping the input power up to higher voltages which equate to the mismatch conditions.

The slides provided in Appendix A illustrate that the improved RF switch, implemented with ACC MOSFETs made in accordance with the present disclosed method and apparatus, has improved large voltage handling capabilities as compared to the prior art RF switch implementations. As shown in the slides, the harmonics are approximately 20 dB at the worst mismatch phase angle. Transient harmonics are also shown. Those skilled in the art shall observe that the standard SP6T switch 3 fo overshoots by several dB before reaching a final value. The improved SP6T switch made in accordance with the present disclosed method and apparatus does not exhibit such a time-dependency.

Slide number 8 of the Appendix A shows insertion loss performance results achieved using the improved SP6T RF switch of the present teachings. It can be observed that the improved SP6T switch has slightly improved insertion loss (IL) performance characteristics. Slide number 9 of Appendix A shows that isolation is also slightly improved using the present improved SP6T RF switch.

Slide number 10 of the Appendix A shows IM3 performance which is a metric of the slightly nonlinear behavior of the RF switch. The IM3 performance is shown versus phase again due to a load mismatch in the system under test. As can be observed by reviewing Slide number 10 of the Appendix A, the performance of the improved SP6T RF switch is improved by 27 dB.

Finally, Slide number 11 of the Appendix A is a summary table which also includes IM2 data. Slide number 11 shows almost 20 dB improvement for a low frequency blocker and 11 dB for a high frequency blocker. In one exemplary application wherein the SP6T may be used, all IM products must fall below −105 dBm. The improved SP6T switch is the only RF switch manufactured at the time of filing the present application meeting this requirement.

A number of embodiments of the present inventive concept have been described. Nevertheless, it will be understood that various modifications may be made without departing from the scope of the inventive teachings. For example, it should be understood that the functions described as being part of one module may in general be performed equivalently in another module. Also, as described above, all of the RF switch circuits can be used in bi-directionally, with output ports used to input signals, and vice versa. Furthermore, the present inventive teachings can be used in the implementation of any circuit that will benefit from the removal of accumulated charge from MOSFET bodies. The present teachings will also find utility in circuits wherein off-state transistors must withstand

relatively high voltages. Other exemplary circuits include DC-to-DC converter circuits, power amplifiers, and similar electronic circuits.

Accordingly, it is to be understood that the concepts described herein are not to be limited by the specific illustrated embodiments, but only by the scope of the appended claims.

What is claimed is:

1. An accumulated charge control (ACC) floating body MOSFET (ACC MOSFET), adapted to control nonlinear response of the MOSFET when the MOSFET is operated in an accumulated charge regime, comprising:

a) a MOSFET having a floating body, wherein the MOSFET is biased to selectively operate in the accumulated charge regime, and wherein accumulated charge is present in the body of the floating body MOSFET when the MOSFET is biased to operate in the accumulated charge regime; and

b) an accumulated charge sink (ACS) operatively coupled to the body of the MOSFET, wherein, when the MOSFET is operated in the accumulated charge regime, an ACS bias voltage (V_{ACS}) is applied to the ACS to control the accumulated charge in the MOSFET body or to remove the accumulated charge from the MOSFET body via the ACS;

wherein the MOSFET includes a gate, drain, source, and a gate oxide layer positioned between the gate and the body, and wherein the MOSFET operates in the accumulated charge regime when the MOSFET is biased to operate in an off-state (non-conducting state), and wherein charge accumulates within the body in a region proximate the gate oxide;

wherein the MOSFET body includes a channel region including a gate modulated conductive channel between the source and the drain, and wherein the source, drain and channel have carriers of identical polarity when the MOSFET is biased to operate in an on-state (conducting state), and wherein the MOSFET operates in the accumulated charge regime when the MOSFET is biased to operate in the off-state and when the accumulated charge has a polarity that is opposite to the polarity of the source, drain and channel carriers.

2. The ACC MOSFET of claim **1**, wherein the MOSFET comprises an NMOSFET device, and wherein the accumulated charge comprises holes having "P" polarity.

3. The ACC MOSFET of claim **2**, wherein the MOSFET comprises an enhancement mode NMOSFET device.

4. The ACC MOSFET of claim **2**, wherein the MOSFET comprises a depletion mode NMOSFET device.

5. The ACC MOSFET of claim **1**, wherein the MOSFET has an inherent linearity characteristic, and wherein the linearity of the ACC MOSFET is improved by removing or otherwise reducing the accumulated charge from the MOSFET body.

6. The ACC MOSFET of claim **1**, wherein the MOSFET has an inherent drain-to-source breakdown voltage (BVDSS) characteristic, and wherein the BVDSS characteristic of the ACC MOSFET is improved by removing or otherwise reducing the accumulated charge from the MOSFET body.

7. The ACC MOSFET of claim **1**, wherein the MOSFET has a drain-to-source off-state capacitance (C_{off}) when operated in the off-state (non-conducting state), and wherein the off-state capacitance (C_{off}) exhibits improved linearity characteristics by removing or otherwise reducing the accumulated charge from the MOSFET body.

8. The ACC MOSFET of claim **7**, wherein the off-state capacitance (C_{off}) has an inherent magnitude, and wherein the magnitude of the off-state capacitance (C_{off}) is decreased by removing or otherwise reducing the accumulated charge from the MOSFET body.

9. The ACC MOSFET of claim **7**, wherein the off-state capacitance (C_{off}) varies over time in a presence of a time varying drain-to-source bias voltage (Vds), and wherein the variations of C_{off} over time are reduced by removing or otherwise reducing the accumulated charge from the MOSFET body.

10. The ACC MOSFET of claim **7**, wherein the off-state capacitance (C_{off}) varies over time as the accumulated charge accumulates in the MOSFET body, and wherein the variations of C_{off} over time are reduced by removing or otherwise reducing the accumulated charge from the MOSFET body.

11. The ACC MOSFET of claim **1**, wherein the ACS has an impedance greater than approximately 10^6 ohms.

12. The ACC MOSFET of claim **1**, wherein the ACS has an impedance less than approximately 10^6 ohms.

13. The ACC MOSFET of claim **1**, wherein the ACC MOSFET has an inherent power handling capability, and wherein the ACC MOSFET is capable of processing input signals having increased power levels by removing or otherwise reducing the accumulated charge from the MOSFET body.

14. An accumulated charge control floating body MOSFET (ACC MOSFET) adapted to control charge accumulated in the body of the MOSFET when the MOSFET is biased to operate in an accumulated charge regime, comprising:

a) a gate, drain, source, floating body, and a gate oxide layer positioned between the gate and the floating body, wherein the ACC MOSFET is biased to operate in the accumulated charge regime when the MOSFET is operated in an off-state (non-conducting state) and charge accumulates within the body in a region proximate and underneath the gate oxide layer; and

b) a first accumulated charge sink (ACS) positioned proximate a first distal end of the floating body, wherein the first ACS is in electrical communication with the floating body, and wherein, when the MOSFET is operated in the accumulated charge regime, an ACS bias voltage (V_{ACS}) is applied to the ACS to control the accumulated charge in the MOSFET body or to remove the accumulated charge from the MOSFET body via the ACS; and

an electrical contact region positioned proximate to and in electrical communication with the first ACS, wherein the electrical contact region facilitates electrical coupling to the first ACS.

15. The ACC MOSFET of claim **14**, wherein the ACC MOSFET comprises an ACC NMOSFET, and wherein the source and drain both comprise N+ doped regions, the floating body and the first ACS both comprise P– doped regions, and the electrical contact region comprises a P+ doped region.

16. The ACC MOSFET of claim **14**, wherein the electrical contact region and the ACS are coextensive.

17. The ACC MOSFET of claim **15**, wherein the floating body and the ACS comprise a combined P– doped region that may be fabricated in a single ion-implementation manufacturing step.

18. The ACC MOSFET of claim **14**, wherein the MOSFET body includes a channel region including a gate modulated conductive channel between the source and the drain, and wherein the source, drain and channel have carriers of identical polarity when the ACC MOSFET is operated in an on-state (conducting state), and wherein the ACC MOSFET operates in the accumulated charge regime when the MOSFET is biased to operate in the off-state and when the accumulated charge has a polarity that is opposite to the polarity of the source, drain and channel carriers.

19. The ACC MOSFET of claim **18**, wherein the ACC MOSFET comprises an NMOSFET device, and wherein the accumulated charge comprises holes having "P" polarity.

20. The ACC MOSFET of claim **18**, wherein the ACC MOSFET has a depleted or partially depleted channel region.

21. The ACC MOSFET of claim **14**, wherein the ACS has an impedance greater than approximately 10^6 ohms.

22. The ACC MOSFET of claim **14**, wherein the ACS is positioned a selected distance away from the source and drain thereby reducing parasitic capacitance effects associated with the ACS.

23. The ACC MOSFET of claim **14**, wherein the ACS is coupled to the body at the first distal end of the floating body thereby reducing parasitic capacitance effects associated with the coupling of the ACS to the floating body.

24. The ACC MOSFET of claim **14**, wherein the floating body has a width exceeding approximately 10 μm.

25. The ACC MOSFET of claim **14**, wherein the ACC MOSFET includes a gate terminal electrically coupled to the gate, a drain terminal electrically coupled to the drain, a source terminal electrically coupled to the source, and an ACS terminal electrically coupled to the ACS.

26. The ACC MOSFET of claim **25**, wherein the gate, drain, source and ACS terminals are coupled to their respective regions via low resistance contact regions.

27. The ACC MOSFET of claim **25**, wherein the ACC MOSFET is biased to operate in the accumulated charge regime by applying selected bias voltages to the source, drain and gate terminals, and wherein accumulated charge is removed or otherwise controlled by coupling the ACS terminal to an accumulated charge sinking mechanism.

28. The ACC MOSFET of claim **27**, wherein the accumulated charge is removed or otherwise controlled by applying a selected bias voltage V_{ACS} to the ACS terminal when the ACC MOSFET operates in the accumulated charge regime.

29. The ACC MOSFET of claim **28**, wherein the ACC MOSFET comprises a depletion mode NMOSFET device, and wherein V_{ACS} is selected to be equal to or more negative than the lesser of the source bias voltage and the drain bias voltage.

30. The ACC MOSFET of claim **14**, wherein the electrical contact region is positioned a selected distance away from the source, drain and body, thereby reducing parasitic capacitance effects associated with the ACS.

31. A four-terminal accumulated charge control floating body MOSFET (ACC MOSFET) device, adapted to control charge accumulated in the body of the MOSFET when the MOSFET is biased to operate in an accumulated charge regime, comprising:

a) a gate, drain, source, floating body, and a gate oxide layer positioned between the gate and the floating body, wherein the ACC MOSFET is biased to operate in the accumulated charge regime when the MOSFET is biased to operate in an off-state (non-conducting state) and charge accumulates within the body in a region proximate and underneath the gate oxide layer;

b) an accumulated charge sink (ACS) positioned proximate a distal end of the floating body, wherein the ACS is in electrical communication with the floating body; and

c) a gate terminal electrically coupled to the gate, a drain terminal electrically coupled to the drain, a source terminal electrically coupled to the source, and an ACS terminal electrically coupled to the ACS;

wherein, when the MOSFET is operated in the accumulated charge regime, an ACS bias voltage (V_{ACS}) is applied to the ACS terminal to control the charge accumulated in the body or to remove the accumulated charge from the body via the ACS terminal.

32. The four-terminal ACC MOSFET of claim **31**, wherein the ACS terminal is coupled to an accumulated charge sinking mechanism.

33. The four-terminal ACC MOSFET of claim **32**, wherein the accumulated charge sinking mechanism produces a selectable accumulated charge sink bias voltage (V_{ACS}), and wherein the V_{ACS} is selected such that the accumulated charge is removed from the body when the ACC MOSFET operates in the accumulated charge regime.

34. The four-terminal ACC MOSFET of claim **33**, wherein the accumulated charge sink bias voltage V_{ACS} is driven by a source having a relatively high impedance.

35. The four-terminal ACC MOSFET of claim **34**, wherein the accumulated charge sink bias voltage V_{ACS} is driven by a source having an impedance greater than approximately 10^6 ohms.

36. The four-terminal ACC MOSFET of claim **33**, wherein the gate, drain and source have associated and respective gate (Vg), drain (Vd) and source (Vs) bias voltages, and wherein the ACS bias voltage V_{ACS} is selected to be equal to or more negative than the lesser of both Vs and Vd, thereby conveying the accumulated rhetorical charge from the body when the MOSFET operates in the accumulated charge regime.

37. The ACC MOSFET of claim **1**, wherein the MOSFET is fabricated in a silicon-on-insulator technology.

38. The ACC MOSFET of claim **14**, wherein when the MOSFET is operated in the accumulated charge regime, the ACS bias voltage (V_{ACS}) is applied to the ACS to remove the accumulated charge from the MOSFET body via the ACS.

39. The ACC MOSFET of claim **31**, wherein when the MOSFET is operated in the accumulated charge regime, the ACS bias voltage (V_{ACS}) is applied to the ACS to remove the accumulated charge from the MOSFET body via the ACS terminal.

* * * * *

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February 01, 2012

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THIS OFFICE OF:

U.S. PATENT: *7,123,898*
ISSUE DATE: *October 17, 2006*

By Authority of the
Under Secretary of Commerce for Intellectual Property
and Director of the United States Patent and Trademark Office

E. BORNETT
Certifying Officer

US007123898B2

(12) **United States Patent**
Burgener et al.

(10) **Patent No.: US 7,123,898 B2**
(45) **Date of Patent: Oct. 17, 2006**

(54) **SWITCH CIRCUIT AND METHOD OF SWITCHING RADIO FREQUENCY SIGNALS**

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(73) Assignee: **Peregrine Semiconductor Corporation**, San Diego, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/922,135**

(22) Filed: **Aug. 18, 2004**

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Related U.S. Application Data

(63) Continuation of application No. 10/267,531, filed on Oct. 8, 2002, now Pat. No. 6,804,502.

(60) Provisional application No. 60/328,353, filed on Oct. 10, 2001.

(51) **Int. Cl.**

H04B 1/28	(2006.01)
H01L 29/76	(2006.01)
H04Q 7/20	(2006.01)
H04M 1/00	(2006.01)

(52) **U.S. Cl.** **455/333**; 455/425; 455/550.1; 257/341

(58) **Field of Classification Search** 455/26.1, 455/78, 333, 425, 550.1, 556.1, 560; 257/280, 257/281, 341, 472

See application file for complete search history.

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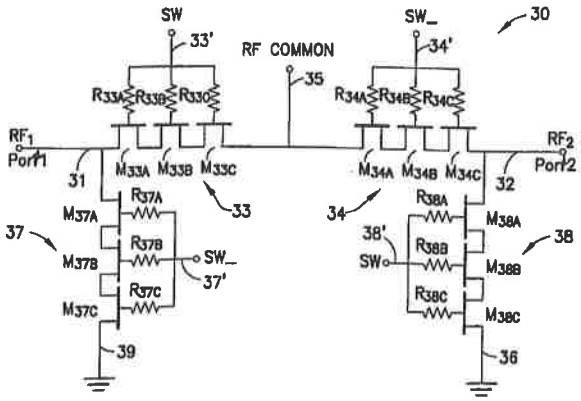
(74) *Attorney, Agent, or Firm*—Jaquez & Associates; Martin J. Jaquez, Esq.

(57) **ABSTRACT**

A novel RF buffer circuit adapted for use with an RF switch circuit and method for switching RF signals is described. The RF switch circuit is fabricated in a silicon-on-insulator (SOI) technology. The RF switch includes pairs of switching and shunting transistor groupings used to alternatively couple RF input signals to a common RF node. The switching and shunting transistor grouping pairs are controlled by a switching control voltage (SW) and its inverse (SW_). The switching and shunting transistor groupings comprise one or more MOSFET transistors connected together in a "stacked" or serial configuration. The stacking of transistor grouping devices, and associated gate resistors, increase the breakdown voltage across the series connected switch transistors and operate to improve RF switch compression. A fully integrated RF switch is described including digital control logic and a negative voltage generator integrated together with the RF switch elements. In one embodiment, the fully integrated RF switch includes a built-in oscillator, a charge pump circuit, CMOS logic circuitry, level-shifting and voltage divider circuits, and an RF buffer circuit. Several embodiments of the charge pump, level shifting, voltage divider, and RF buffer circuits are described. The inventive RF switch provides improvements in insertion loss, switch isolation, and switch compression.

20 Claims, 13 Drawing Sheets



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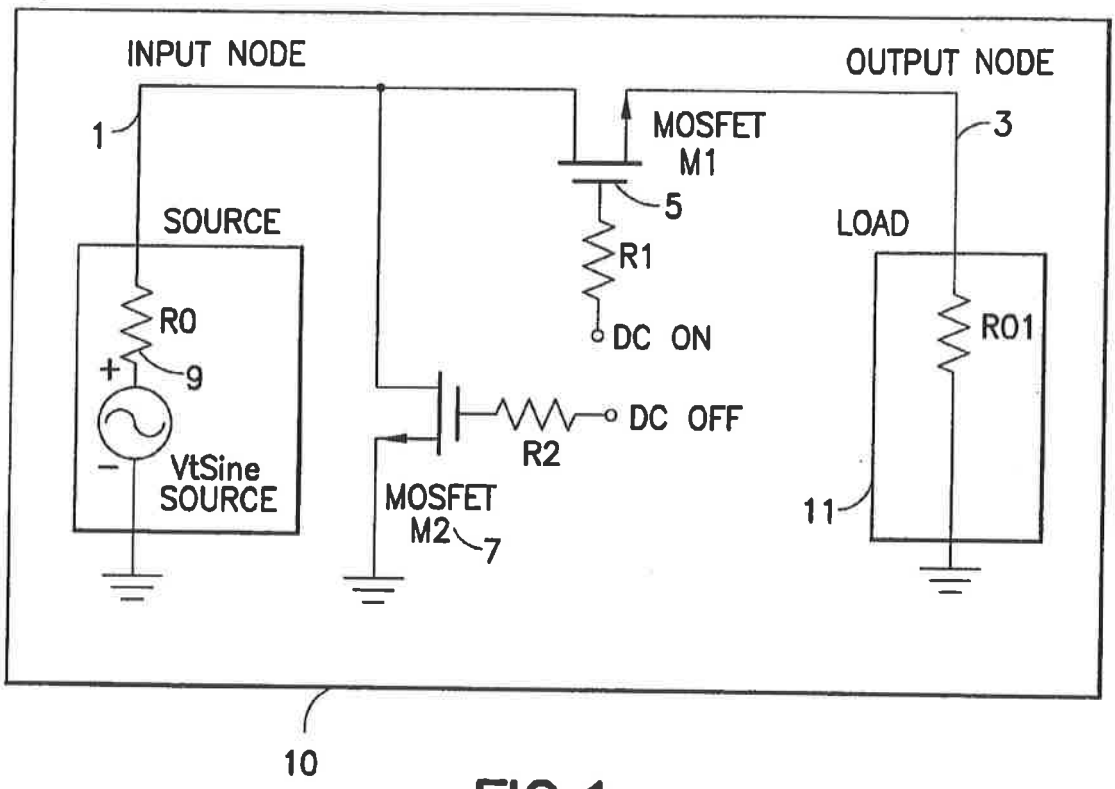

FIG.1a

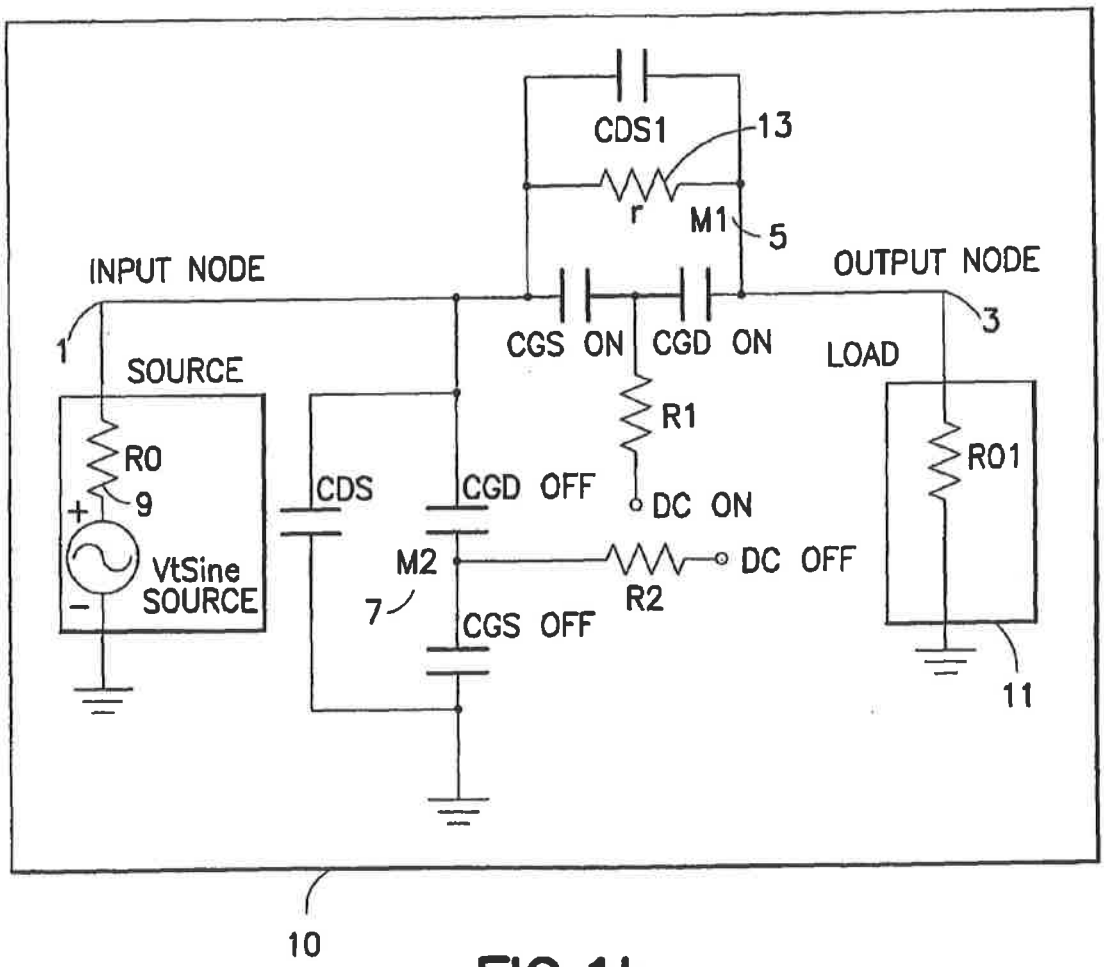

FIG.1b

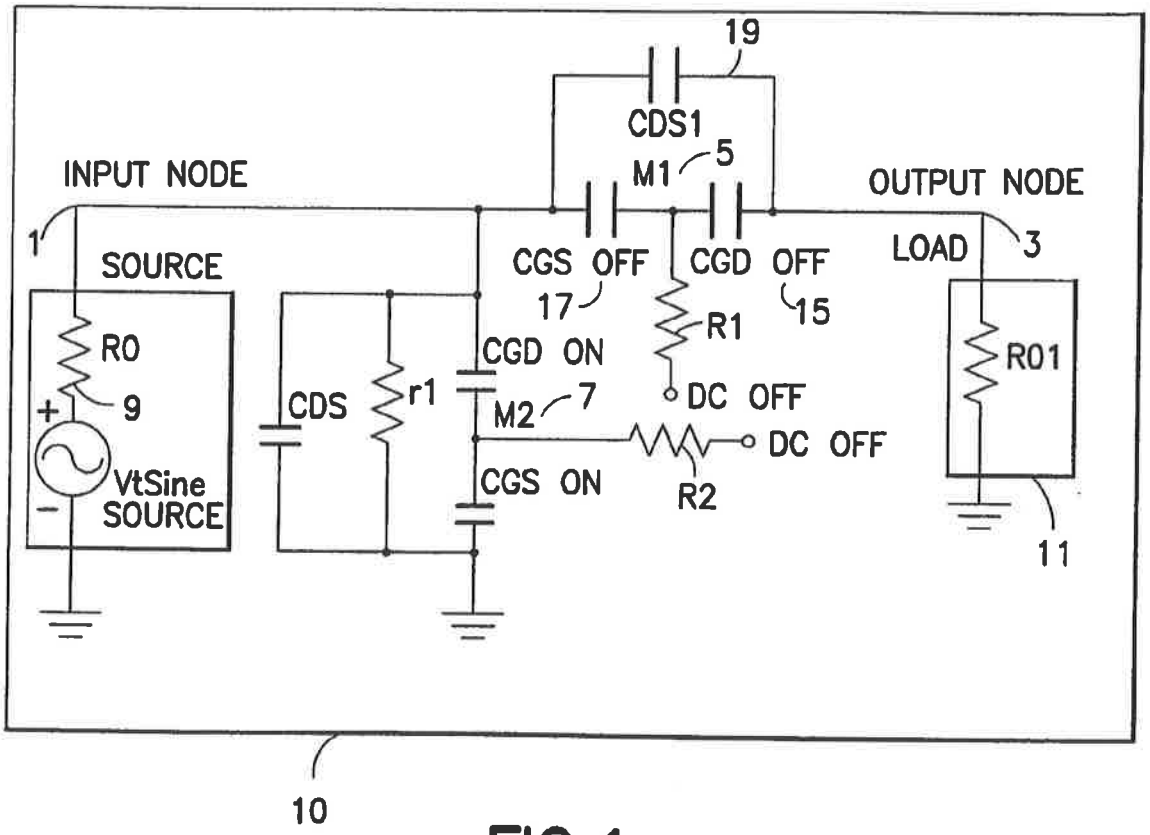

FIG. 1c

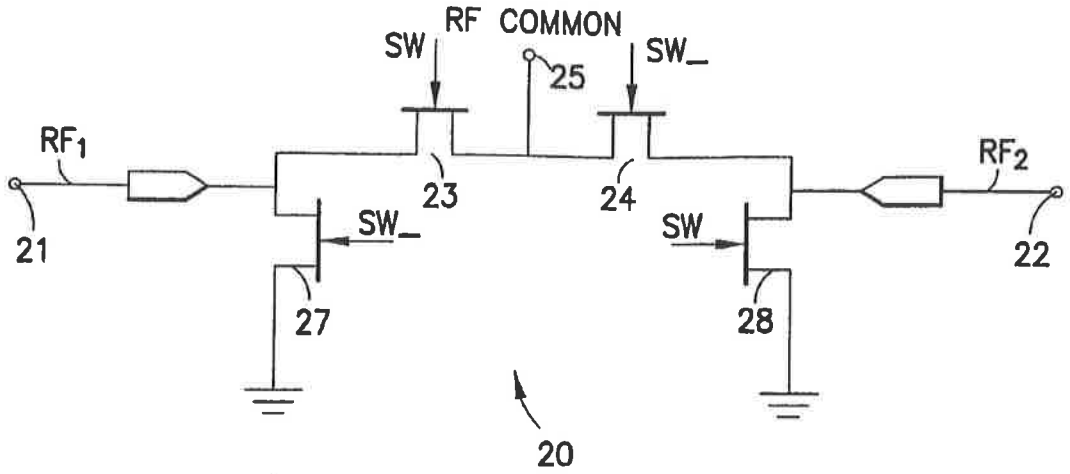

FIG.2

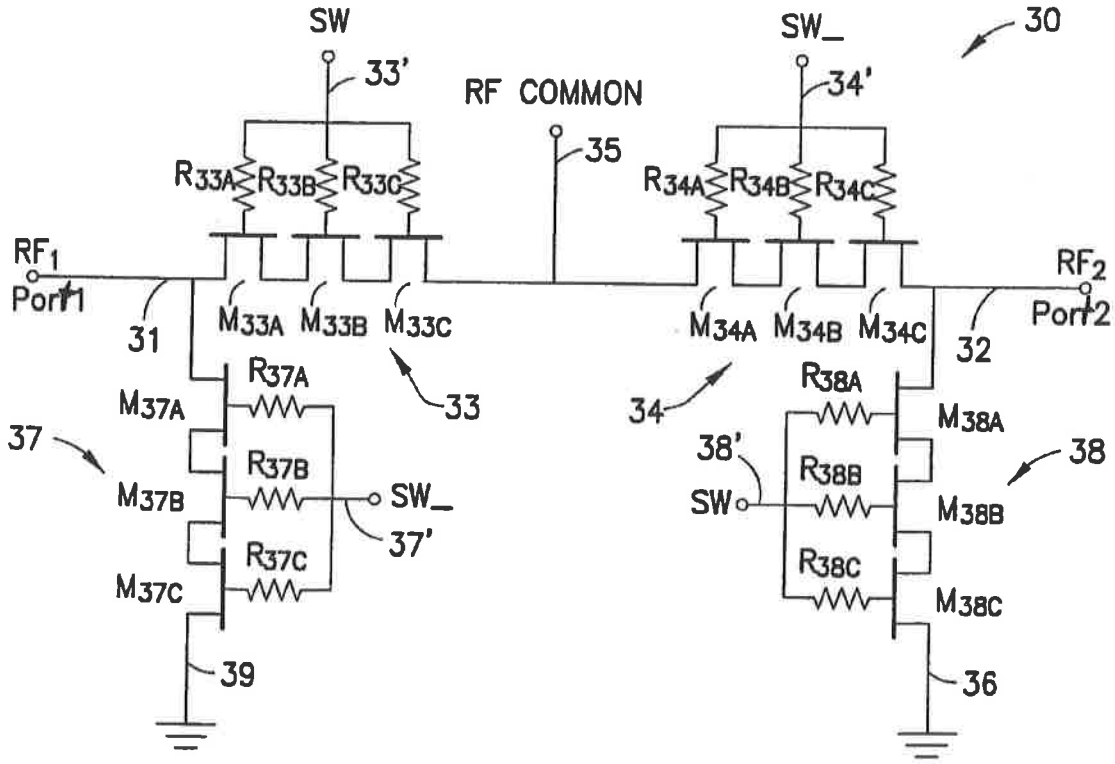

FIG.3

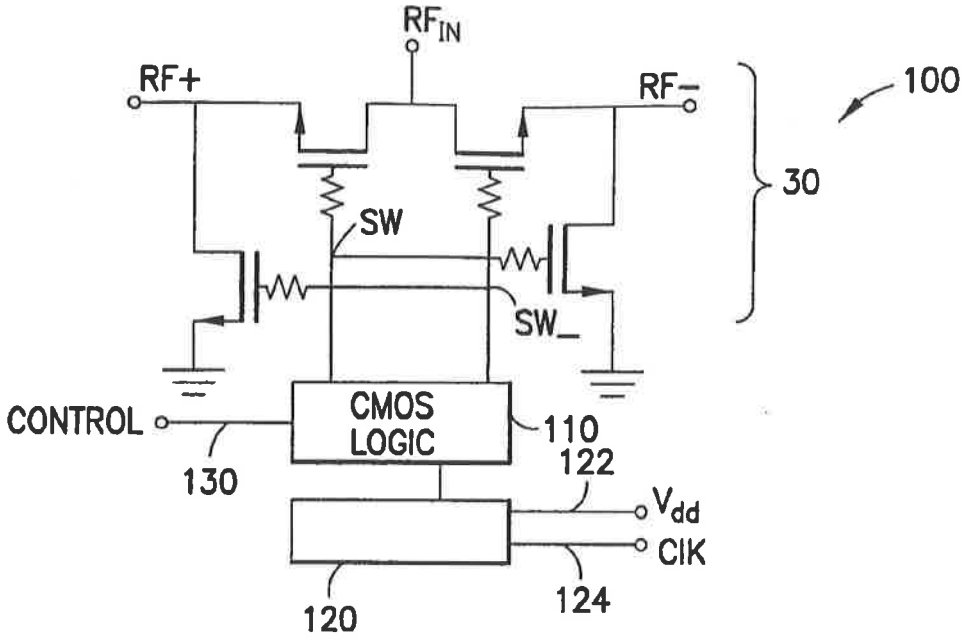

FIG.4

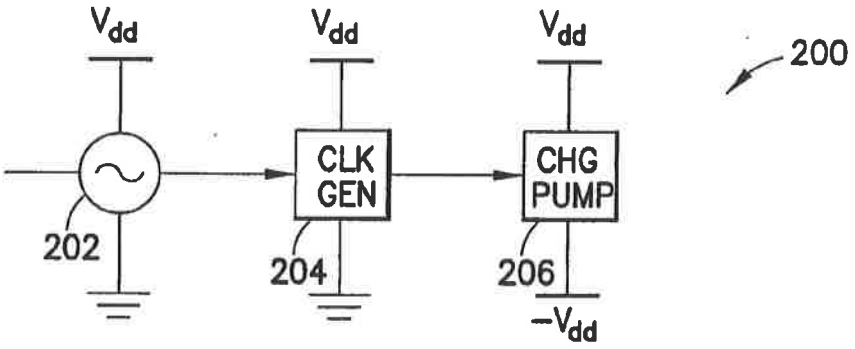

FIG.5a

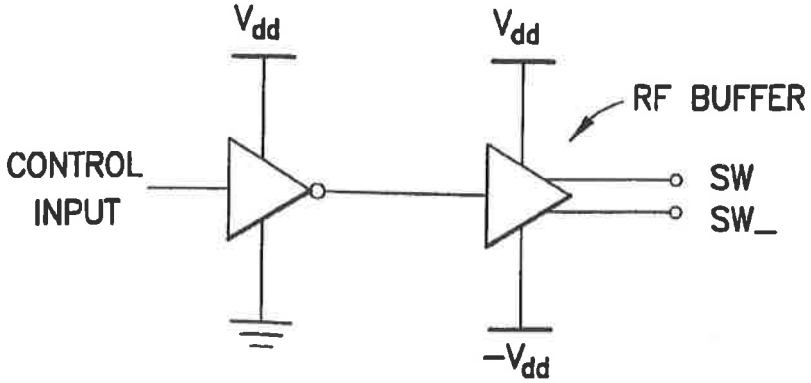

FIG.8b

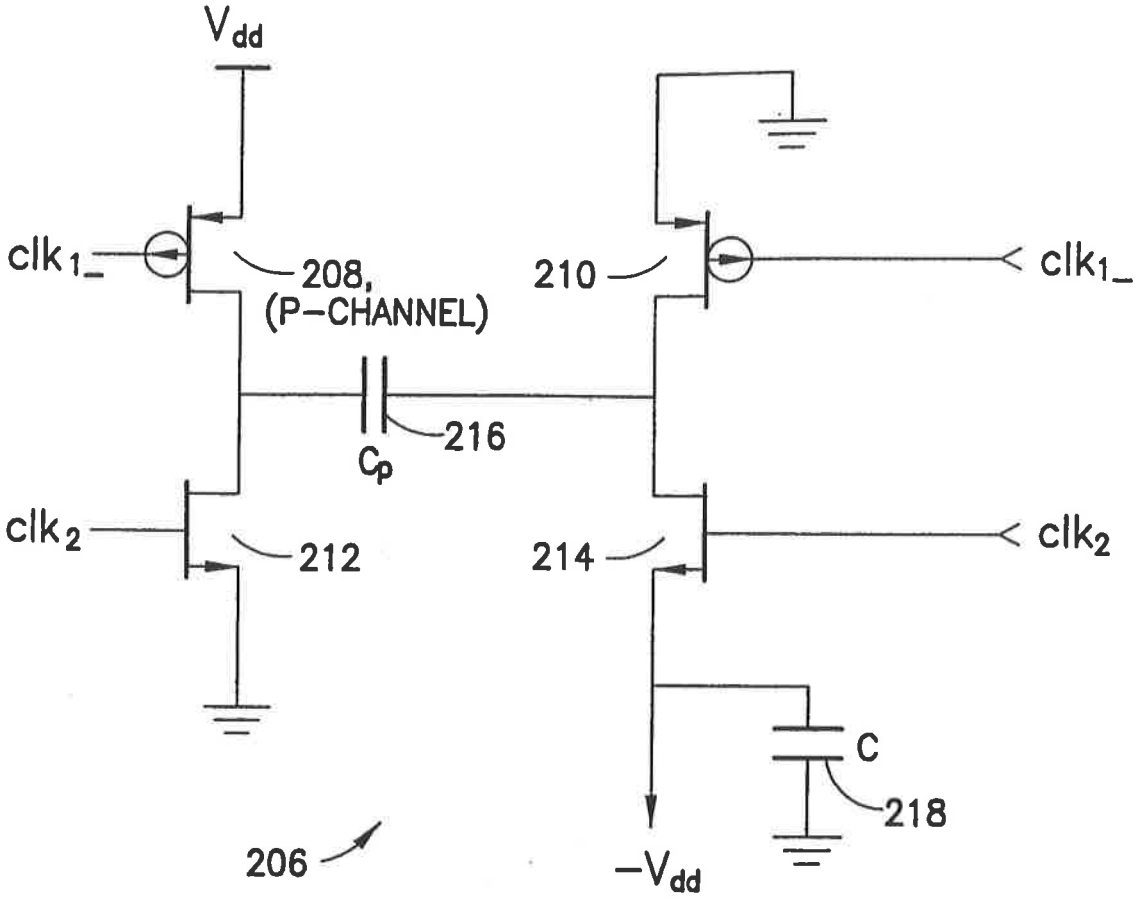

FIG.5b

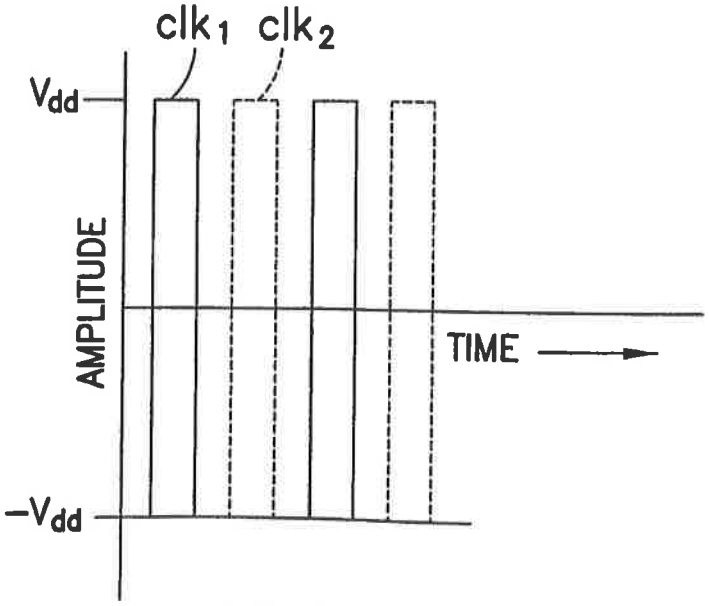

FIG.5c

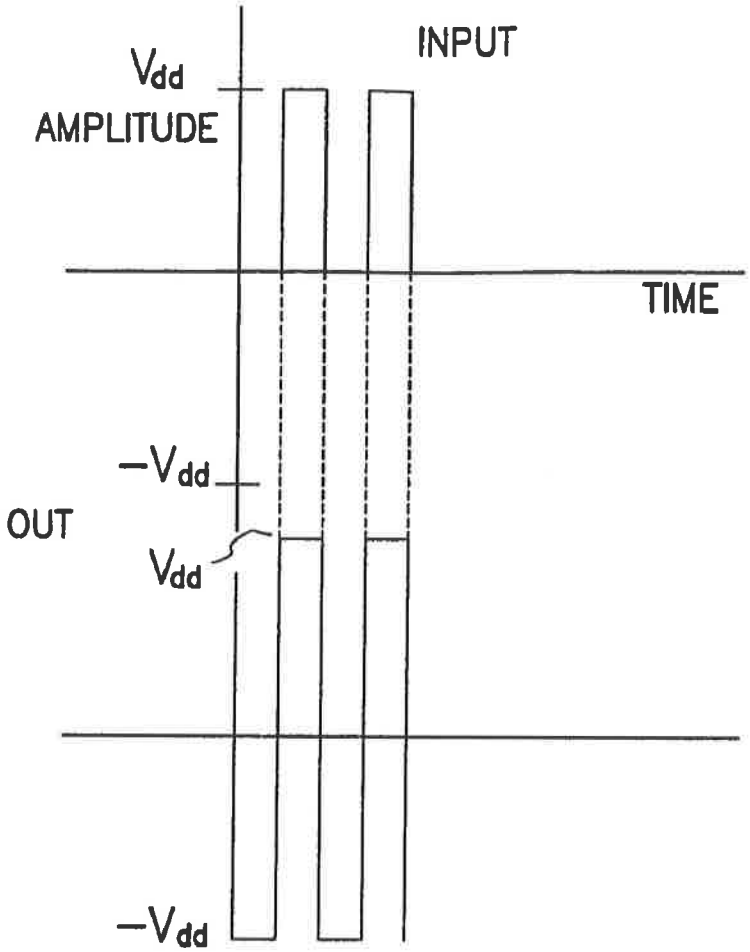

FIG.7a

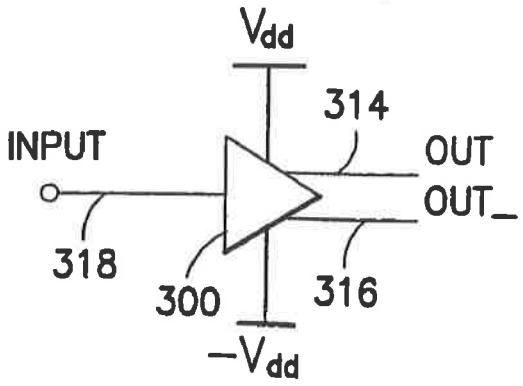

FIG.7b

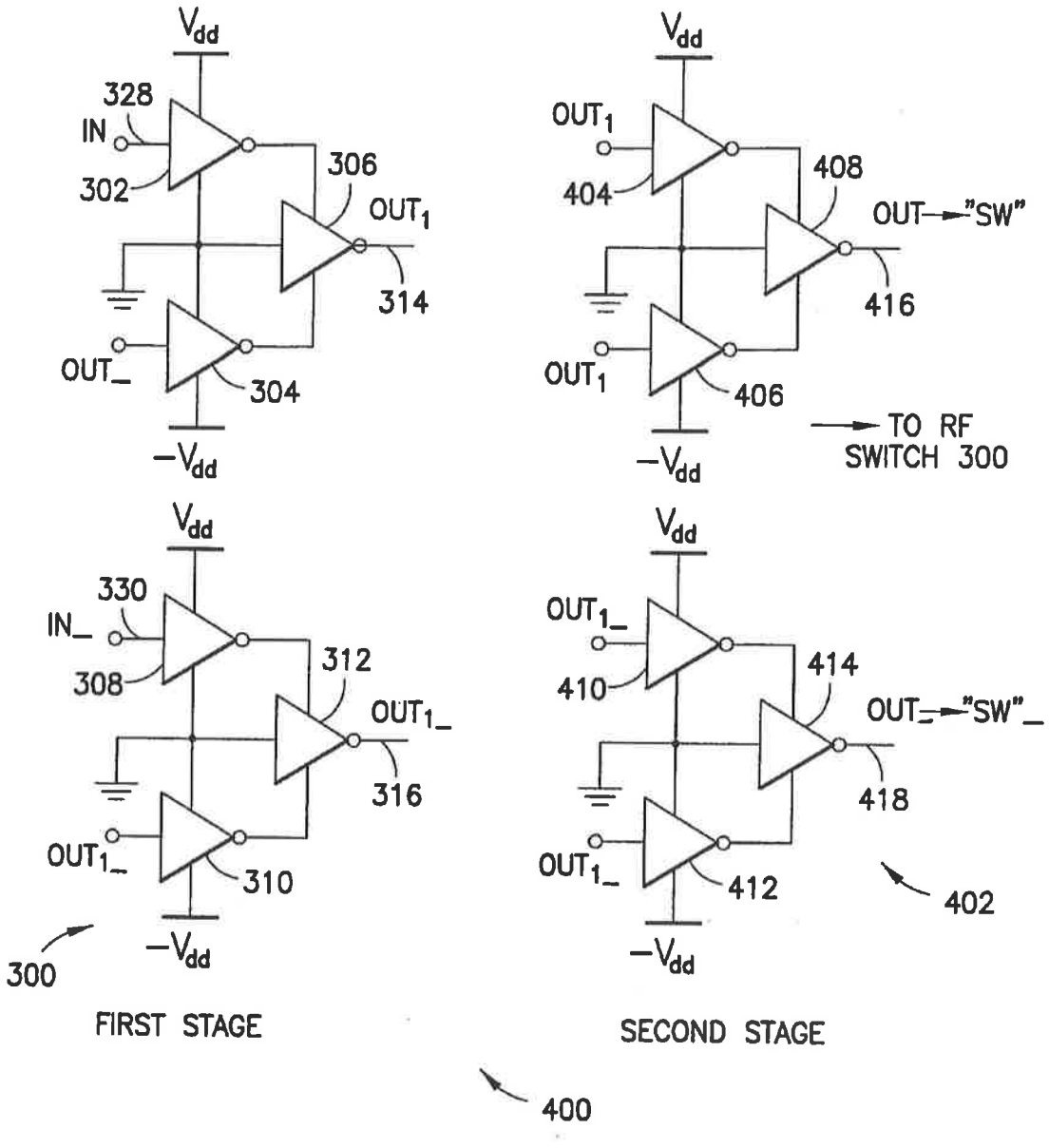

FIG.8a

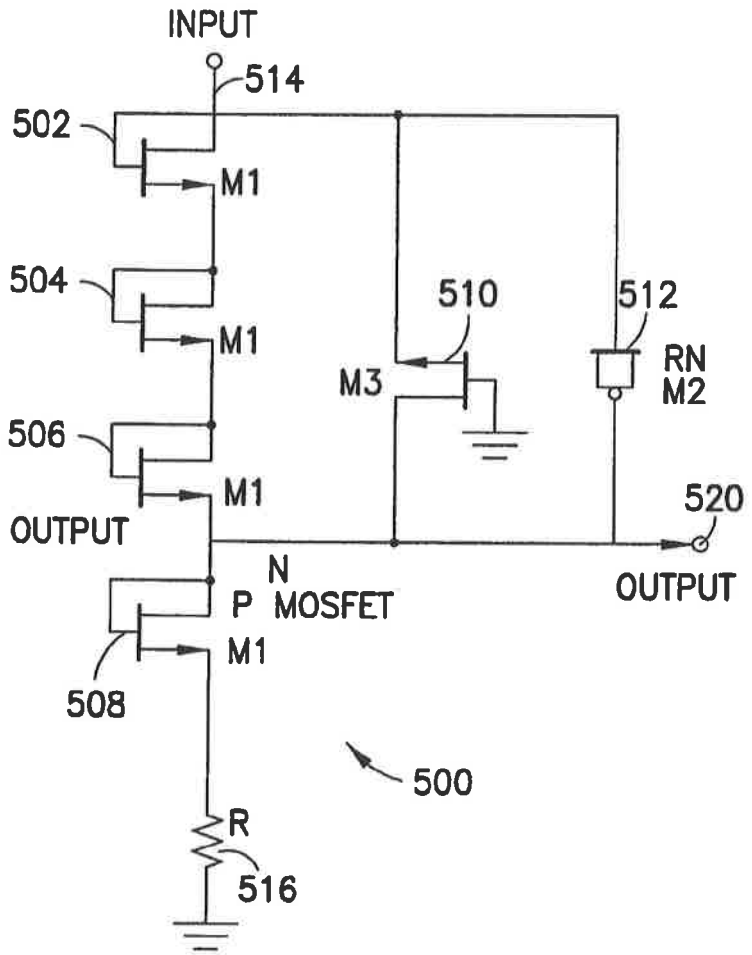

FIG.9a

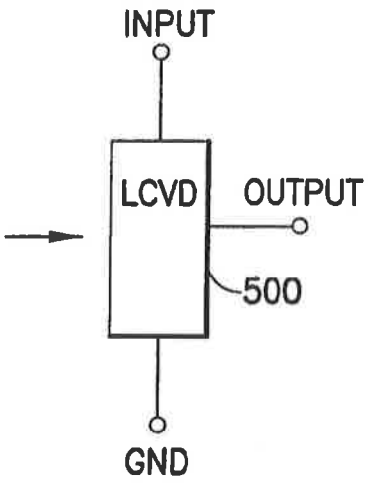

FIG.9b

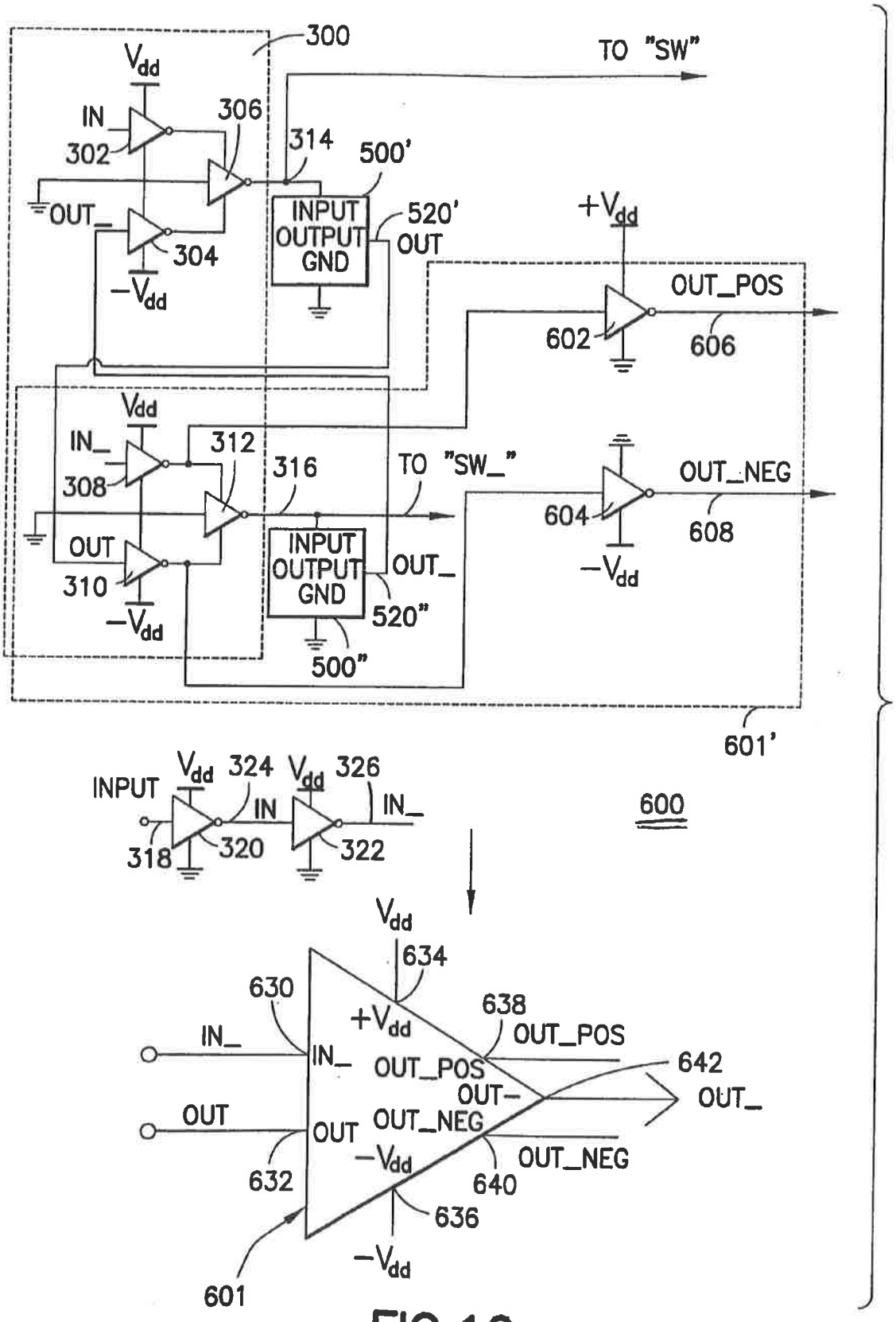

FIG.10

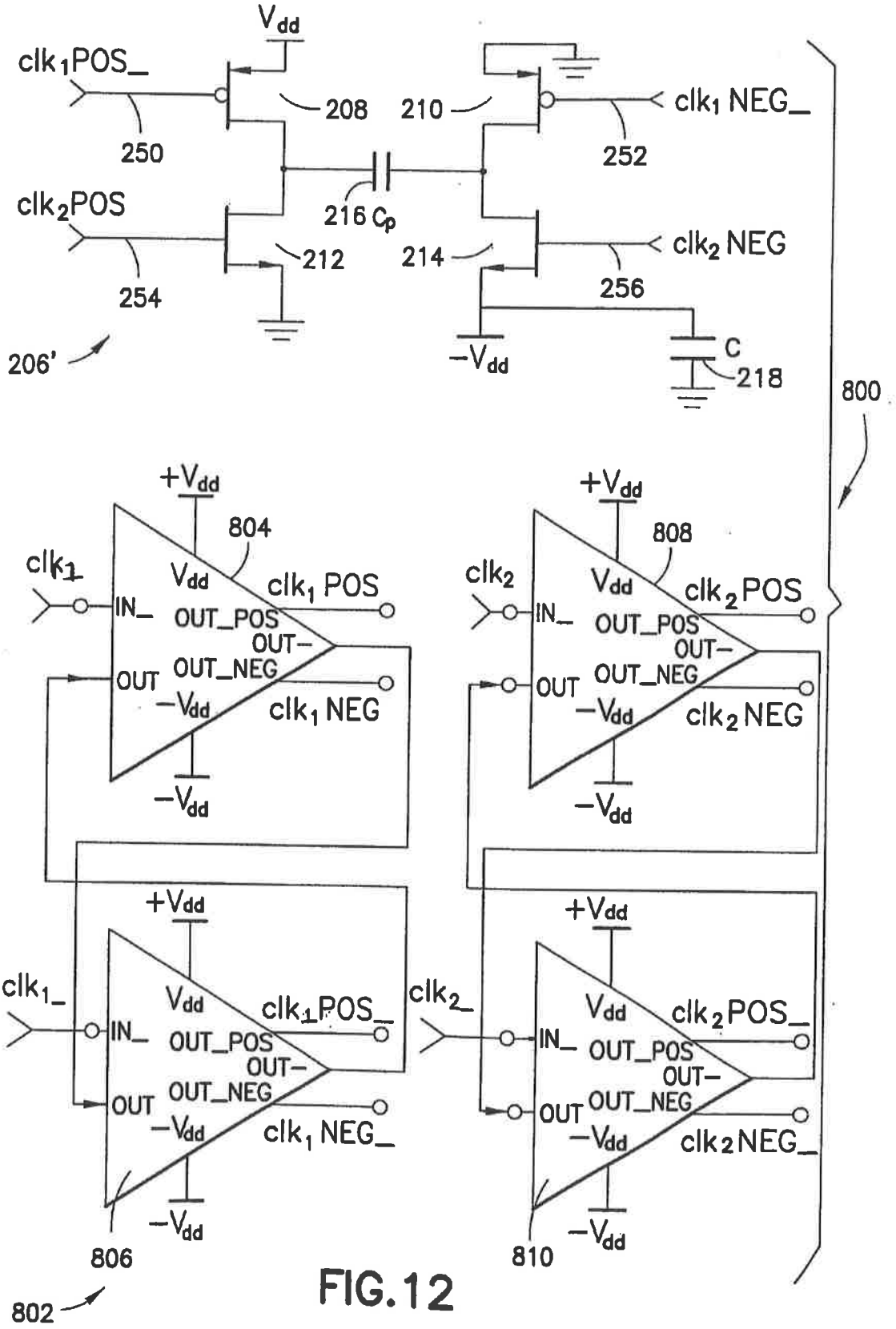

FIG.12

SWITCH CIRCUIT AND METHOD OF SWITCHING RADIO FREQUENCY SIGNALS

CROSS-REFERENCE TO RELATED UTILITY AND PROVISIONAL APPLICATIONS—CLAIM OF PRIORITY UNDER 35 USC SECTIONS 120 AND 119(e)

This is a continuation application of application Ser. No. 10/267,531, filed Oct. 8, 2002, now U.S. Pat. No. 6,805,502, which claims the benefit of U.S. Provisional Application No. 60/328,353, filed Oct. 10, 2001. Both the parent application (U.S. application Ser. No. 10/267,531, filed Oct. 8, 2002) and the related provisional application (U.S. Provisional Application No. 60/328,353 , filed Oct. 10, 2001) are incorporated by reference herein in their entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to switches, and particularly to a switch circuit and method of switching radio frequency (RF) signals within an integrated circuit. In one embodiment, the switch circuit comprises CMOS devices implemented on a silicon-on-insulator (SOI) substrate, for use in RF applications such as wireless communications, satellites, and cable television.

2. Description of Related Art

As is well known, radio frequency (RF) switches are important building blocks in many wireless communication systems. RF switches are found in many different communications devices such as cellular telephones, wireless pagers, wireless infrastructure equipment, satellite communications equipment, and cable television equipment. As is well known, the performance of RF switches is controlled by three primary operating performance parameters: insertion loss, switch isolation, and the "1 dB compression point." These three performance parameters are tightly coupled, and any one parameter can be emphasized in the design of RF switch components at the expense of others. A fourth performance parameter that is occasionally considered in the design of RF switches is commonly referred to as the switching time or switching speed (defined as the time required to turn one side of a switch on and turn the other side off). Other characteristics that are important in RF switch design include ease and degree (or level) of integration of the RF switch, complexity, yield, return loss and cost of manufacture.

These RF switch performance parameters can be more readily described with reference to a prior art RF switch design shown in the simplified circuit schematics of FIGS. **1***a*–**1***c*. FIG. **1***a* shows a simplified circuit diagram of a prior art single pole, single throw (SPST) RF switch **10**. The prior art SPST switch **10** includes a switching transistor M1 **5** and a shunting transistor M2 **7**. Referring now to FIG. **1***a*, depending upon the state of the control voltages of the two MOSFET transistors M1 **5** and M2 **7** (i.e., depending upon the DC bias applied to the gate inputs of the MOSFET switching and shunting transistors, M1 and M2, respectively), RF signals are either routed from an RF input node **1** to an RF output node **3**, or shunted to ground through the shunting transistor M2 **7**. Actual values of the DC bias voltages depend upon the polarity and thresholds of the MOSFET transistors M1 **5** and M2 **7**. Resistor R0 **9**, in series with the RF source signal, isolates the bias from the source signal and is essential for optimal switch performance. FIG. **1***b* shows the "on" state of the RF switch **10** of FIG. **1***a* (i.e.,

FIG. **1***b* shows the equivalent small-signal values of the transistors M1 and M2 when the RF switch **10** is "on", with switching transistor M1 **5** on, and shunting transistor M2 **7** off). FIG. **1***c* shows the "off" state of the switch **10** of FIG. **1***a* (i.e., FIG. **1***c* shows the equivalent small-signal values of the transistors M1 and M2 when the RF switch **10** is "off", with switching transistor M1 **5** off, and shunting transistor M2 **7** on).

As shown in FIG. **1***b*, when the RF switch **10** is on, the switching transistor M1 **5** is primarily resistive while the shunting transistor M2 **7** is primarily capacitive. The "insertion loss" of the RF switch **10** is determined from the difference between the maximum available power at the input node **1** and the power that is delivered to a load **11** at the output node **3**. At low frequencies, any power lost is due to the finite on resistance "r" **13** of the switching transistor M1 **5** when the switch **10** is on (see FIG. **1***b*). The on resistance r **13** (FIG. **1***b*) typically is much less than the source resistor R0 **9**. The insertion loss, "IL", can therefore be characterized in accordance with Equation 1 shown below:

$$IL \text{ is approximately equal to: } 10r/R0\ \ln(10)=0.087r \text{ (in dB).} \qquad \text{Equation 1}$$

Thus, at low frequencies, a 3-Ω value for r results in approximately 0.25 dB insertion loss. Because insertion loss depends greatly upon the on resistances of the RF switch transmitters, lowering the transistor on resistances and reducing the parasitic substrate resistances can achieve improvements in insertion loss.

In general, the input-to-output isolation (or more simply, the switch isolation) of an RF switch is determined by measuring the amount of power that "bleeds" from the input port into the output port when the transistor connecting the two ports is off. The isolation characteristic measures how well the RF switch turns off (i.e., how well the switch blocks the input signal from the output). More specifically, and referring now to the "off" state of the RF switch **10** of FIG. **1***c*, the switching transistor M1 **5** off state acts to block the input **1** from the output **3**. The shunting transistor M2 **7** also serves to increase the input-to-output isolation of the switch **10**.

When turned off (i.e., when the RF switch **10** and the switching transistor M1 **5** are turned off), M1 **5** is primarily capacitive with "feedthrough" (i.e., passing of the RF input signal from the input node **1** to the output node **3**) of the input signal determined by the series/parallel values of the capacitors CGD off **15** (Gate-to-Drain Capacitance when the switching transistor M1 is turned off), CGS off **17** (Gate-to-Source Capacitance when the switching transistor M1 is turned off), and CDS1 **19** (Drain-to-Source capacitance when the transistor M1 is turned off). Feedthrough of the input signal is undesirable and is directly related to the input-to-output isolation of the RF switch **10**. The shunting transistor M2 **7** is used to reduce the magnitude of the feedthrough and thereby increase the isolation characteristic of the RF switch.

The shunting transistor M2 **7** of FIG. **1***c* is turned on when the switching transistor M1 **5** is turned off. In this condition, the shunting transistor M2 **7** acts primarily as a resistor having a value of r. By design, the value of r is much less than the characteristic impedance of the RF source. Consequently, r greatly reduces the voltage at the input of the switching transistor M1 **5**. When the value of r is much less than the source resistance R0 **9** and the feedthrough capacitive resistance of the shunting transistor M2 **7**, isolation is easily calculated. Switch isolation for the off state of the RF

switch **10** is determined as the difference between the maximum available power at the input to the power at the output.

In addition to RF switch insertion loss and isolation, another important RF switch performance characteristic is the ability to handle large input power when the switch is turned on to ensure that insertion loss is not a function of power at a fixed frequency. Many applications require that the switch does not distort power transmitted through a "switched-on" switch. For example, if two closely spaced tones are concurrently passed through an RF switch, non-linearities in the switch can produce inter-modulation (IM) and can thereby create a false tone in adjacent channels. If these adjacent channels are reserved, for instance, for information signals, power in these false tones must be maintained as small as possible. The switch compression, or "1 dB compression point" ("P1dB"), is indicative of the switch's ability to handle power. The P1 dB is defined as the input power at which the insertion loss has increased by 1 dB from its low-power value. Or stated in another way, the 1 dB compression point is a measure of the amount of power that can be input to the RF switch at the input port before the output power deviates from a linear relationship with the input power by 1 dB.

Switch compression occurs in one of two ways. To understand how switch compression occurs, operation of the MOSFET transistors shown in the RF switch **10** of FIGS. **1***a*–**1***c* are described. As is well known in the transistor design arts, MOSFETs require a gate-to-source bias that exceeds a threshold voltage, V_t, to turn on. Similarly, the gate-to-source bias must be less than V_t for the switch to be off. V_t is positive for "type-N" MOSFETs and negative for "type-P" MOSFETs. Type-N MOSFETs were chosen for the RF switch **10** of FIGS. **1***a*–**1***c*. The source of a type-N MOSFET is the node with the lowest potential.

Referring again to FIG. **1***c*, if a transient voltage on the shunting transistor M2 **7** results in turning on the shunting transistor M2 **7** during part of an input signal cycle, input power will be routed to ground and lost to the output. This loss of power increases for increased input power (i.e., input signals of increased power), and thereby causes a first type of compression. The 1 dB compression point in the RF switch **10** is determined by the signal swing on the input at which point the turned-off shunting transistor M2 **7** is unable to remain off. Eventually, a negative swing of the input falls below the potential of the M2 gate, as well as below ground (thus becoming the source). When this difference becomes equal to V_t, the transistor M2 **7** begins to turn on and compression begins. This first type of compression is caused by the phenomenon of the turning on of a normally off gate in the shunt leg of the RF switch. Once the shunting transistor M2 **7** turns on, power at the output node **3** no longer follows power at the switch input in a linear manner. A second type of RF switch compression occurs when the source and drain of the shunting transistor M2 **7** break down at excessive voltages. For submicron silicon-on-insulator (SOI) devices, this voltage may be approximately only +1 VDC above the supply voltage. At breakdown, the shunt device begins to heavily conduct current thereby reducing the power available at the output.

FIG. **2** shows a simplified schematic of a prior art single pole double throw (SPDT) RF switch **20**. As shown in FIG. **2**, the prior art RF switch **20** minimally includes four MOSFET transistors **23**, **24**, **27** and **28**. The transistors **23** and **24** act as "pass" or "switching" transistors (similar to the switching MOSFET transistor M1 **5** of FIGS. **1***a*–**1***c*), and are configured to alternatively couple their associated and respective RF input nodes to a common RF node **25**. For example, when enabled (or switched "on"), the switching transistor **23** couples a first RF input signal "RF_1", input to a first RF input node **21**, to the RF common node **25**. Similarly, when enabled, the switching transistor **24** couples a second RF input signal "RF_2", input to a second RF input node **22**, to the RF common node **25**. The shunting transistors, **27** and **28**, when enabled, act to alternatively shunt their associated and respective RF input nodes to ground when their associated RF input nodes are uncoupled from the RF common node **25** (i.e., when the switching transistor (**23** or **24**) connected to the associated input node is turned off).

As shown in FIG. **2**, two control voltages are used to control the operation of the prior art RF switch. The control voltages, labeled "SW", and its inverse "SW_", control the operation of the transistors **23**, **24**, **27** and **28**. The control voltages are arranged to alternatively enable (turn on) and disable (turn off) selective transistor pairs. For example, as shown in FIG. **2**, when SW is on (in some embodiments this is determined by the control voltage SW being set to a logical "high" voltage level, e.g., "+Vdd"), the switching transistor **23** is enabled, and its associated shunting transistor **28** is also enabled. However, because the inverse of SW, SW_, controls the operation of the second switching transistor **24**, and its associated shunting transistor **27**, and the control signal SW_ is off during the time period that SW is on (in some embodiments this is determined by SW_ being set to a –Vdd value), those two transistors are disabled, or turned off, during this same time period. In this state (SW "on" and SW_ "off"), the RF_1 input signal is coupled to the RF common port **25** (through the enabled switching transistor **23**). Because the second switching transistor **24** is turned off, the RF_2 input signal is blocked from the RF common port **25**. Moreover, the RF_2 input signal is further isolated from the RF common port **25** because it is shunted to ground through the enabled shunting transistor **28**. As those skilled in the transistor designs arts shall easily recognize, the RF_2 signal is coupled to the RF common port **25** (and the RF_1 signal is blocked and shunted to ground) in a similar manner when the SW control signal is "off" (and SW_ is "on").

With varying performance results, RF switches, such as the SPDT RF switch **20** of FIG. **2**, have heretofore been implemented in different component technologies, including bulk complementary-metal-oxide-semiconductor (CMOS) and gallium-arsenide (GaAs) technologies. In fact, most high performance high-frequency switches use GaAs technology. The prior art RF switch implementations attempt to improve the RF switch performance characteristics described above, however, they do so with mixed results and with varying degrees of integrated circuit complexity and yields. For example, bulk CMOS RF switches disadvantageously exhibit high insertion loss, low compression, and poor linearity performance characteristics. In contrast, due to the semi-insulating nature of GaAs material, parasitic substrate resistances can be greatly reduced thereby reducing RF switch insertion loss. Similarly, the semi-insulating GaAs substrate improves switch isolation.

Although GaAs RF switch implementations offer improved performance characteristics, the technology has several disadvantages. For example, GaAs technology exhibits relatively low yields of properly functioning integrated circuits. GaAs RF switches tend to be relatively expensive to design and manufacture. In addition, although GaAs switches exhibit improved insertion loss characteristics as described above, they may have low frequency limitations due to slow states present in the GaAs substrate.

The technology also does not lend itself to high levels of integration, which requires that digital control circuitry associated with the RF switch be implemented "off chip" from the switch. The low power control circuitry associated with the switch has proven difficult to integrate. This is disadvantageous as it both increases the overall system cost or manufacture, size and complexity, as well as reducing system throughput speeds.

It is therefore desirable to provide an RF switch and method for switching RF signals having improved performance characteristics. Specifically, it is desirable to provide an RF switch having improved insertion loss, isolation, and compression. It is desirable that such an RF switch be easily designed and manufactured, relatively inexpensive to manufacture, lend itself to high levels of integration, with low-to-high frequency application. Power control circuitry should be easily integrated on-chip together with the switch functions. Such integration has been heretofore difficult to achieve using Si and GaAs substrates. The present invention provides such an RF switch and method for switching RF signals.

SUMMARY OF THE INVENTION

A novel RF switch circuit and method for switching RF signals is described. The RF switch circuit may be used in wireless applications, and may be fabricated in a silicon-on-insulator technology. In one embodiment the RF switch is fabricated on an Ultra-Thin-Silicon ("UTSi") substrate. In one embodiment the RF switch includes: an input for receiving an RF signal; a first switching transistor grouping connected to the input to receive the RF signal and connected to an RF common port, wherein the first switching transistor is controlled by a switching voltage (SW); a second switching transistor grouping connected to the first switching transistor grouping and the RF common port, wherein the second switching transistor is controlled by a switching voltage SW_, and wherein SW_ is the inverse of SW so that when the first switching transistor grouping is on, the second switching transistor grouping is off. The switching transistor groupings, when enabled, alternatively connect their respective RF input signals to the RF common port. In this embodiment the RF switch also includes shunting transistor groupings coupled to the switching transistor groupings and also controlled by the switching voltages SW and SW_. The shunting transistor groupings, when enabled, act to alternatively shunt their associated RF input nodes to ground thereby improving RF switch isolation.

The switching and shunting transistor groupings comprise one or more MOSFET transistors connected together in a "stacked" or serial configuration. Within each transistor grouping, the gates of the stacked transistors are commonly controlled by a switching voltage (SW or SW_) that is coupled to each transistor gate through respective gate resistors. The stacking of transistor grouping devices and gate resistors increases the compression point of the switch. The RC time constant formed by the gate resistors and the gate capacitance of the MOSFETs is designed to be much longer than the period of the RF signal, causing the RF voltage to be shared equally across the series connected devices. This configuration increases the 1 dB compression point of the RF switch.

A fully integrated RF switch is described that includes digital switch control logic and a negative power supply voltage generator circuit integrated together with the inventive RF switch. In one embodiment, the fully integrated RF switch provides several functions not present in prior art RF switches. For example, in one embodiment, the fully integrated RF switch includes a built-in oscillator that provides clocking input signals to a charge pump circuit, an integrated charge pump circuit that generates the negative power supply voltages required by the other RF switch circuits, CMOS logic circuitry that generates control signals to control the RF switch transistors, level-shifting and low current voltage divider circuits that provide increased reliability of the switch devices, and an RF buffer circuit that isolates RF signal energy from the charge pump and digital control logic circuits. Several embodiments of the charge pump, level shifting, voltage divider, and RF buffer circuits are described. The inventive RF switch provides improvements in insertion loss, switch isolation, and switch compression. In addition, owing to the higher levels of integration made available by the present inventive RF switch, RF system design and fabrication costs are reduced and reliability is increased using the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1***a* is a simplified electrical schematic of a prior art single pole, single throw (SPST) RF switch used to demonstrate performance characteristics of the RF switch.

FIG. **1***b* is a simplified electrical schematic of the SPST RF switch of FIG. **1***a* showing the dominant characteristics of the switch when the switch is turned "on" allowing the RF signal to pass from an input node to an output node.

FIG. **1***c* shows the equivalent small-signal electrical characteristics of the RF switch of FIGS. **1***a* and **1***b* when the RF switch is turned "off" thereby blocking the RF signal from the output node.

FIG. **2** is a simplified electrical schematic of a prior art single pole double throw (SPDT) RF switch.

FIG. **3** is an electrical schematic of an RF switch according to one embodiment of the present invention.

FIG. **4** is a simplified block diagram of an exemplary fully integrated RF switch made in accordance with the present invention.

FIG. **5***a* is a simplified block diagram of one exemplary embodiment of the negative voltage generator shown in the simplified block diagram of FIG. **4**; FIG. **5***b* is an electrical schematic of a first embodiment of a charge pump circuit that is used to generate a negative supply voltage to the RF switch of FIG. **4**.

FIG. **5***c* is a plot of voltage amplitude versus time showing the voltage amplitude of two non-overlapping clock signals used to control the charge pump circuit of FIG. **5***b* varying over time.

FIG. **6***a* is an electrical schematic of a first embodiment of an inventive level shifting circuit; FIG. **6***b* is an electrical schematic of one embodiment of the inverters used to implement the level shifter shown in FIG. **6***a*.

FIG. **7***a* is a voltage amplitude versus time plot of a digital input signal and corresponding output signal generated by the inventive level shifter of FIG. **6***a*; FIG. **7***b* is a simplified logic symbol for the inventive level shifter of FIG. **6***a*.

FIG. **8***a* is an electrical schematic of one embodiment of a two-stage level shifter and RF buffer circuit including a first stage level shifter and a second stage RF buffer circuit; FIG. **8***b* is a simplified block diagram of the digital control input and interface to the RF buffer circuit of FIG. **8***a*.

FIG. **9***a* is an electrical schematic of one embodiment of a low current voltage divider (LCVD) circuit made in accordance with the present RF switch invention; FIG. **9***b* is a simplified logic symbol used to represent the voltage divider of FIG. **9***a*.

FIG. **10** is an electrical schematic of a second embodiment of a level shifting circuit using the low current voltage divider circuit of FIG. **9***a* in combination with the level shifting circuit of FIG. **6***a*.

FIGS. **11***a* and **11***b* are electrical schematics showing an alternative embodiment of the two-stage level shifter and RF buffer circuit of FIG. **8***a*.

FIG. **12** is an electrical schematic of a modified charge pump using the level shifting circuit of FIG. **10**.

Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION OF THE INVENTION

Throughout this description, the preferred embodiment and examples shown should be considered as exemplars, rather than as limitations on the present invention.

The Inventive RF Switch

The present invention is a novel RF switch design and method for switching RF circuits. A first exemplary embodiment of the present inventive RF switch **30** is shown in FIG. **3**. As shown in FIG. **3**, in one embodiment, the inventive RF switch **30** includes four clusters or "groupings" of MOSFET transistors, identified in FIG. **3** as transistor groupings **33**, **34**, **37** and **38**. Two transistor groupings comprise "pass" or "switching" transistor groupings **33** and **34**, and two transistor groupings comprise shunting transistor groupings **37** and **38**. Each transistor grouping includes one or more MOSFET transistors arranged in a serial configuration. For example, in the embodiment shown in FIG. **3**, the switching grouping **33** includes three switching transistors, M_{33A}, M_{33B}, and M_{33C}. Similarly, the switching grouping **34** includes three switching transistors, M_{34A}, M_{34B}, and M_{34C}. The shunting grouping **37** includes three transistors M_{37A}, M_{37B}, and M_{37C}. Similarly, the shunting grouping **38** includes three transistors, M_{38A}, M_{38B}, and M_{38C}. Although the transistor groupings **33**, **34**, **37** and **38** are shown in FIG. **3** as comprising three MOSFET transistors, those skilled in the RF switch design arts shall recognize that alternative grouping configurations can be used without departing from the scope or spirit of the present invention. For example, as described below in more detail, any convenient number of transistors can be used to implement the groupings shown in FIG. **3** without departing from the scope of the present invention.

In one embodiment of the present inventive RF switch, the MOSFET transistors (e.g., the transistors M_{37A}, M_{37B}, and M_{37C}) are implemented using a fully insulating substrate silicon-on-insulator (SOI) technology. More specifically, and as described in more detail hereinbelow, the MOSFET transistors of the inventive RF switch are implemented using "Ultra-Thin-Silicon (UTSi)" (also referred to herein as "ultrathin silicon-on-sapphire") technology. In accordance with UTSi manufacturing methods, the transistors used to implement the inventive RF switch are formed in an extremely thin layer of silicon in an insulating sapphire wafer. The fully insulating sapphire substrate enhances the performance characteristics of the inventive RF switch by reducing the deleterious substrate coupling effects associated with non-insulating and partially insulating substrates. For example, improvements in insertion loss are realized by lowering the transistor on resistances and by reducing parasitic substrate resistances. In addition, switch isolation is improved using the fully insulating substrates provided by UTSi technology. Owing to the fully insulating nature of silicon-on-sapphire technology, the parasitic capacitance between the nodes of the RF switch **30** are greatly reduced as compared with bulk CMOS and other traditional integrated circuit manufacturing technologies. Consequently, the inventive RF switch exhibits improved switch isolation as compared with the prior art RF switch designs.

As shown in FIG. **3**, similar to the switch described above with reference to FIG. **2**, the transistor groupings are controlled by two control signals, SW, and its inverse, SW_. The control signals are coupled to the gates of their respective transistors through associated and respective gate resistors. For example, the control signal SW controls the operation of the three transistors in the switching transistor grouping **33** (M_{33A}, M_{33B}, and M_{33C}) through three associated and respective gate resistors (R_{33A}, R_{33B}, and R_{33C}, respectively). The control signal SW is input to an input node **33'** to control the switching transistor grouping **33**. SW is also input to an input node **38'** to control the shunting transistor grouping **38**. Similarly, the inverse of SW, SW_, controls the switching transistor grouping **34** via an input node **34'**. SW_ is also input to an input node **37'** to control the shunting transistor grouping **37**.

In one embodiment, the transistor grouping resistors comprise approximately 30 K ohm resistors, although alternative resistance values can be used without departing from the spirit or scope of the present invention. In addition, in some embodiments of the present invention, the gate resistors comprise any resistive element having a relatively high resistance value. For example, reversed-biased diodes may be used to implement the gate resistors in one embodiment. As described in more detail below, the gate resistors help to increase the effective breakdown voltage across the series connected transistors.

The control signals function to control the enabling and disabling of the transistor groupings **33**, **34**, **37** and **38**, and the RF switch **30** generally functions to pass and block RF signals in a manner that is similar to the control of the analogous transistors of the switch of FIG. **2**. More specifically, the switching transistor groupings **33** and **34** act as pass or switching transistors, and are configured to alternatively couple their associated and respective RF input nodes to a common RF node **35**. For example, when enabled, the switching transistor grouping **33** couples a first RF input signal "RF_1", input to a first RF input node **31**, to the RF common node **35**. Similarly, when enabled, the switching transistor grouping **34** couples a second RF input signal "RF_2", input to a second RF input node **32**, to the RF common node **35**. The shunting transistor groupings, **37** and **38**, when enabled, act to alternatively shunt their associated and respective RF input nodes to ground when their associated RF input nodes are uncoupled from the RF common node **35** (i.e., when the switching transistor grouping (**33** or **34**) that is connected to the associated input node is turned off).

The control voltages are connected to alternatively enable and disable selective pairs of transistor groupings. For example, as shown in FIG. **3**, when SW is on (in some embodiments this is determined when the control voltage SW is set to a logical "high" voltage level), the switching transistor grouping **33** is enabled (i.e., all of the transistors in the grouping **33** are turned on), and its associated shunting transistor grouping **38** is also enabled (i.e., all of the transistors in the grouping **38** are turned on). However, similar to the operation of the switch of FIG. **2**, because the inverse of SW, SW_, controls the operation of the second switching transistor grouping **34**, and its associated shunting transistor grouping **37**, these two transistors groupings are disabled

(i.e., all of the transistors in the groupings **34**, **37** are turned off) during this time period. Therefore, with SW on, the RF_1 input signal is coupled to the RF common port **35**. The RF_2 input signal is blocked from the RF common port **35** because the switching transistor grouping **34** is off. The RF_2 input signal is further isolated from the RF common port **35** because it is shunted to ground through the enabled shunting transistor grouping **38**. As those skilled in the RF switch design arts shall recognize, the RF_2 signal is coupled to the RF common port **35** (and the RF_1 , signal is blocked and shunted to ground) in a similar manner when the SW control signal is off (and the SW_ control signal is on).

One purpose of the stacking of MOSFET transistors and using gate resistors as shown in the inventive RF switch **30** of FIG. **3** is to increase the breakdown voltage across the series connected transistors. The RC time constant formed by the gate resistor and the gate capacitance of the MOSFETs is designed to be much longer than the period of the RF signal. Thus, very little RF energy is dissipated through the gate resistor. This arrangement effectively causes the RF voltage to be shared equally across the series connected transistors. The net effect is that the breakdown voltage across the series connected devices is increased to n times the breakdown voltage of an individual FET, where n is the number of transistors connected in series. This configuration increases the 1 dB compression point of the inventive RF switch **30**.

To achieve improved switch performance, the RC time constant must be sized so that it is large with respect to the period of the RF signal. This largely places a constraint on the minimum value of R that can be used to implement the gate transistors. As noted above, in one embodiment of the present invention, a typical value of R is 30 k-ohms, although other resistance values can be used without departing from the scope of the present invention. Because a MOSFET gate input draws no DC current, there is no change in the biasing of the devices due to IR drops across this resistance.

Advantageously, the present inventive RF switch **30** can accommodate input signals of increased power levels. Owing to the serial arrangement of the MOSFET transistors that comprise the transistor groupings (**33**, **34**, **37** and **38**), increased power signals can be presented at the RF input nodes (i.e., at the input nodes **31** and **32**) without detrimentally affecting switch operation. Those skilled in the transistor design arts art shall recognize that greater input power levels can be accommodated by increasing the number of transistors per transistor grouping, or by varying the physical configuration of the transistors. For example, in one embodiment, the transistors are approximately 0.5×2,100 micro-meters in dimension. However, alternative configurations can be used without departing from the scope or spirit of the present invention.

Silicon-on-Insulator (SOI) Technologies

As noted above in the description of the RF switch of FIG. **3**, SOI technology is attractive in implementing RF switches due to the fully insulating nature of the insulator substrate. As is well known, SOI has been used in the implementation of high performance microelectronic devices, primarily in applications requiring radiation hardness and high speed operation. SOI technologies include, for example, SIMOX, bonded wafers having a thin silicon layer bonded to an insulating layer, and silicon-on-sapphire. In order to achieve the desired switch performance characteristics described above, in one embodiment, the inventive RF switch is fabricated on a sapphire substrate.

Fabrication of devices on an insulating substrate requires that an effective method for forming silicon CMOS devices on the insulating substrate be used. The advantages of using a composite substrate comprising a monocrystalline semiconductor layer, such as silicon, epitaxially deposited on a supporting insulating substrate, such as sapphire, are well-recognized, and can be realized by employing as the substrate an insulating material, such as sapphire (Al_2O_3), spinel, or other known highly insulating materials, and providing that the conduction path of any inter-device leakage current must pass through the substrate.

An "ideal" silicon-on-insulator wafer can be defined to include a completely monocrystalline, defect-free silicon layer of sufficient thickness to accommodate the fabrication of active devices therein. The silicon layer would be adjacent to an insulating substrate and would have a minimum of crystal lattice discontinuities at the silicon-insulator interface. Early attempts to fabricate this "ideal" silicon-on-insulator wafer were frustrated by a number of significant problems, which can be summarized as (1) substantial incursion of contaminants into the epitaxially deposited silicon layer, especially the p-dopant aluminum, as a consequence of the high temperatures used in the initial epitaxial silicon deposition and the subsequent annealing of the silicon layer to reduce defects therein; and (2) poor crystalline quality of the epitaxial silicon layers when the problematic high temperatures were avoided or worked around through various implanting, annealing, and/or re-growth schemes.

It has been found that the high quality silicon films suitable for demanding device applications can be fabricated on sapphire substrates by a method that involves epitaxial deposition of a silicon layer on a sapphire substrate, low temperature ion implant to form a buried amorphous region in the silicon layer, and annealing the composite at temperatures below about 950° C.

Examples of and methods for making such silicon-on-sapphire devices are described in U.S. Pat. No. 5,416,043 ("Minimum charge FET fabricated on an ultrathin silicon on sapphire wafer"); U.S. Pat. No. 5,492,857 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); U.S. Pat. No. 5,572,040 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); U.S. Pat. No. 5,596,205 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); U.S. Pat. No. 5,600,169 ("Minimum charge FET fabricated on an ultrathin silicon on sapphire wafer"); U.S. Pat. No. 5,663,570 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); U.S. Pat. No. 5,861,336 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); U.S. Pat. No. 5,863,823 ("Self-aligned edge control in silicon on insulator"); U.S. Pat. No. 5,883,396 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); U.S. Pat. No. 5,895,957 ("Minimum charge FET fabricated on an ultrathin silicon on sapphire wafer"); U.S. Pat. No. 5,920,233 ("Phase locked loop including a sampling circuit for reducing spurious side bands"); U.S. Pat. No. 5,930,638 ("Method of making a low parasitic resistor on ultrathin silicon on insulator"); U.S. Pat. No. 5,973,363 ("CMOS circuitry with shortened P-channel length on ultrathin silicon on insulator"); U.S. Pat. No. 5,973,382 ("Capacitor on ultrathin semiconductor on insulator"); and U.S. Pat. No. 6,057,555 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"). All of these referenced patents are incorporated herein in their

entirety for their teachings on ultrathin silicon-on-sapphire integrated circuit design and fabrication.

Using the methods described in the patents referenced above, electronic devices can be formed in an extremely thin layer of silicon on an insulating synthetic sapphire wafer. The thickness of the silicon layer is typically less than 150 nm. Such an "ultrathin" silicon layer maximizes the advantages of the insulating sapphire substrate and allows the integration of multiple functions on a single integrated circuit. Traditional transistor isolation wells required for thick silicon are unnecessary, simplifying transistor processing and increasing circuit density. To distinguish these above-referenced methods and devices from earlier thick-silicon embodiments, they are herein referred to collectively as "ultrathin silicon-on-sapphire."

In some preferred embodiments of the invention, the MOS transistors are formed in ultrathin silicon-on-sapphire wafers by the methods disclosed in U.S. Pat. Nos. 5,416,043; 5,492,857; 5,572,040; 5,596,205; 5,600,169; 5,663,570; 5,861,336; 5,863,823; 5,883,396; 5,895,957; 5,920,233; 5,930,638; 5,973,363; 5,973,382; and 6,057,555. However, other known methods of fabricating ultrathin silicon-on-sapphire integrated circuits can be used without departing from the spirit or scope of the present invention.

As described and claimed in these patents, high quality silicon films suitable for demanding device applications can be fabricated on insulating substrates by a method that involves epitaxial deposition of a silicon layer on an insulating substrate, low temperature ion implantation to form a buried amorphous region in the silicon layer, and annealing the composite at temperatures below about 950° C. Any processing of the silicon layer which subjects it to temperatures in excess of approximately 950° C. is performed in an oxidizing ambient environment. The thin silicon films in which the transistors are formed typically have an areal density of electrically active states in regions not intentionally doped which is less than approximately $5.\times10^{11}$ cm^{-2}.

As noted above, UTSi substrates are especially desirable for RF applications because the fully insulating substrate reduces the detrimental effects of substrate coupling associated with traditional substrates (i.e., substrates that are not fully insulating). Consequently, in one embodiment, the RF switch **30** of FIG. **3** is fabricated on an UTSi substrate.

RF Switch Design Tradeoffs

Several design parameters and tradeoffs should be considered in designing and implementing the inventive RF switch **30** described above with reference to FIG. **3**. The inventive RF switch can be tailored to meet or exceed desired system design requirements and RF switch performance objectives. The design tradeoffs and considerations that impact the inventive RF switch design are now described.

As described above with reference to FIG. **3**, the RF switch **30** is implemented using MOSFET transistors, which may be "N-type" or "P-type". However, N channel transistors are preferred for RF switches implemented in CMOS technology. N channel transistors are preferred because, for a given transistor size, the "on" resistance of an N channel transistor is much lower than for a P channel transistor due to the higher mobility in silicon of electrons versus holes. The control voltages are selected to insure that the on resistance of the "on" transistor is reduced. The control voltages are also selected to insure that the "off" transistor remains off when disabled.

As is well known in the transistor design arts, in an N channel MOS transistor, the "on" resistance is inversely proportional to the difference between the voltage applied at the transistor gate and the voltage applied at the transistor source. This voltage is commonly referred to as the "Vgs" (gate-to-source voltage). It is readily observed that as the magnitude of the RF signal (Vs) increases at the input port (e.g., at the first RF input node **31** of FIG. **3**), and hence at the RF common port **35**, the Vgs of the on transistors decrease (e.g., the Vgs of the transistor $M33_A$ in the switching transistor grouping **33** decreases as the magnitude of the RF **1** signal increases). This argues for making the gate control voltage (e.g., SW at the input node **33'**) as positive as possible. Unfortunately, reliability concerns limit the extent to which the gate control voltage can be made positive.

A similar concern exists for the "off" transistors. It is important to note that for typical RF switch applications, the RF input signals (e.g., the RF **1** input signal) generally swing about a zero reference voltage. The off transistors (e.g., the transistors in the shunting transistor grouping **37**) must remain disabled or turned off during both the positive and negative voltage excursions of the RF input signal. This argues for making the gate control voltage of the off transistors (e.g., the SW_ control voltage signal) as negative as possible. Again, reliability concerns limit the extent to which this gate control voltage can be made negative.

For a CMOS switch, the design of the off transistor also limits the 1 dB compression point of the switch. As is well known in the transistor design arts, MOS transistors have a fundamental breakdown voltage between their source and drain. When the potential across the device exceeds this breakdown voltage, a high current flows between source and drain even when a gate potential exists that is attempting to keep the transistor in an off state. Improvements in switch compression can be achieved by increasing the breakdown voltage of the transistors. One method of fabricating a MOS transistor with a high breakdown voltage is to increase the length of the gate. Unfortunately, an increase in gate length also disadvantageously increases the channel resistance of the device thereby increasing the insertion loss of the device. The channel resistance can be decreased by making the device wider, however this also decreases the switch isolation. Hence, tradeoffs exist in MOS switch designs.

As described above with reference to the inventive RF switch **30** of FIG. **3**, the transistors are stacked in a series configuration to improve the switch 1 dB compression point. The relatively high value gate resistors, in combination with the stacking configuration of the transistors in the transistor groupings, increase the effective breakdown voltage across the series connected transistors. The switch elements are designed and fabricated such that the RC time constant (determined by the resistance values of the gate resistors and the gate capacitance of the MOSFETs) is much longer than the period of the RF signal processed by the RF switch **30**. As noted above, the net effect of the stacking configuration and the relatively high resistance gate resistors is to increase the breakdown voltage across the series connected transistors by a factor of n times the breakdown voltage of an individual transistor (where n equals the number of transistors connected in series in a transistor grouping).

An additional design consideration concerns the "body tie" used in traditional bulk CMOS transistors. As is well known in the transistor design arts, the body tie electrically couples the device either to the well or to the substrate. The well-substrate junction must remain reversed biased at all times. The source-to-body and drain-to-body junctions must remain reversed biased at all times. In general, for bulk CMOS designs, the well (for N-well technology) is tied to

the most positive potential that will be applied to the circuit. The substrate (for P-well technology) is tied to the most negative potential that will be applied to the circuit. Because the RF input signal swings symmetrically above and below ground, bulk CMOS switch designs exhibit poor insertion loss, isolation, and 1 dB compression point performance. For these reasons, and those described above, the present RF switch **30** is preferably implemented on an insulating substrate.

Implementing the inventive RF switch on an insulating substrate provides several advantages such as improved switch isolation and reduced insertion loss. Further advantages are achieved by implementing the inventive RF switch using UTSi technology. For example, as compared with the prior art RF switch implementations in GaAs, improvements in integrated circuit yields, reduced fabrication costs, and increased levels of integration are achieved using UTSi. As is well known in the integrated circuit design arts, GaAs does not lend itself to high levels of integration. Thus, the digital control circuitry and other circuitry associated with the operation and function of the RF switch (such as a negative voltage power supply generator, level shifting, low current voltage divider and RF buffer circuits) must often be implemented off-chip (i.e., these functions are not easily integrated with the RF switch). This leads to increased costs and reduced performance of the prior art RF switch implementations.

In contrast, in accordance with the present RF switch invention, using UTSi technology, the circuitry necessary for the proper operation and functioning of the RF switch can be integrated together on the same integrated circuit as the switch itself. For example, and as described below in more detail, by implementing the RF switch in UTSi technology, the RF switch can be integrated in the same integrated circuit with a negative voltage generator and the CMOS control logic circuitry required to control the operation of the RF switch. The complexity of the RF switch is also reduced owing to the reduction in control lines required to control the operation of the switch. Advantageously, the RF switch control logic can be implemented using low voltage CMOS transistors. In addition, even for high power RF switch implementations, a single, relatively low power external power supply can be used to power the present inventive RF switch. This feature is advantageous as compared to the prior art GaAs implementations that require use of a relatively high power external power supply and power generation circuitry necessary to generate both positive and negative power supplies. For example, in the exemplary embodiments described below with reference to FIGS. **4–12**, the present inventive RF switch requires only a single 3 V external power supply. The prior art switch designs typically require at least a 6 volt external power supply, and external voltage generation circuitry to generate both positive and negative power supplies.

Fully Integrated RF Switch

FIG. **4** shows a simplified block diagram of an exemplary fully integrated RF switch **100** made in accordance with the present invention. As shown in FIG. **4**, the fully integrated RF switch **100** includes the inventive RF switch **30** described above in FIG. **3** (shown in a simplified schematic representation in FIG. **4**), CMOS control logic **110**, and a negative voltage generator circuit **120** (implemented in one embodiment using a "charge pump" circuit). A control signal **130** is input to the CMOS logic block **110**. In one embodiment, the control signal **130** ranges from 0 volts to +Vdd, however those skilled in the digital logic design arts shall recognize that other logic levels can be used without departing from the scope or spirit of the present invention. For the reasons provided above, in one exemplary embodiment, the fully integrated RF switch **100** is fabricated on UTSi substrates, although other insulating substrate technologies can be used.

As described in more detail below, the fully integrated RF switch **100** includes several functions and features not present in the prior art RF switch of FIG. **2**. For example, in addition to the inventive RF switch **30** (which makes use of the novel transistor stacking and gate transistor configuration described above with reference to FIG. **3**), the fully integrated RF switch **100** integrates the negative voltage generator and RF switch control functions together on the same integrated circuit as the inventive RF switch. As described below in more detail, the fully integrated RF switch **100** includes a built-in oscillator that provides clocking input signals to a charge pump circuit, an integrated charge pump circuit that generates the negative power supply voltages required by the other RF switch circuits, CMOS logic circuitry that generates the control signals that control the RF switch transistors, a level-shifting circuit that provides increased reliability by reducing the gate-to-drain, gate-to-source, and drain-to-source voltages of the switch transistors, and an RF buffer circuit that isolates RF signal energy from the charge pump and digital control logic circuits. Each of these circuits is described below in more detail with reference to their associated figures.

Negative Voltage Generator—Charge Pump—A First Embodiment

As shown in FIG. **4**, one embodiment of the fully integrated RF switch **100** includes a negative voltage generator or charge pump **120**. The negative voltage generator **120** generates the negative power supply voltage (specified hereafter as "−Vdd") required by other circuits of the fully integrated RF switch **100**. Two sets of inputs are provided to the negative voltage generator **120**: a positive DC power supply voltage signal (Vdd) **122**; and a clocking input (shown in the figure as a single input signal, "Clk") **124**. Although the clocking input **124** is shown as a single input signal in FIG. **4**, as described below with reference to FIG. **5***b*, in some embodiments of the present inventive RF switch, the clocking input **124** may comprise two or more clock input signals.

In addition, in the embodiment shown in FIG. **4**, the positive supply voltage that is input to the negative voltage generator circuit **120** comprises a 3 VDC power supply. However, other power supply levels may be used without departing from the scope or spirit of the present invention. For example, if desired, a 3.5 VDC, 5 VDC or any other convenient positive DC power supply can be input to the negative voltage generator circuit **120** of FIG. **4**. The positive power supply signal is typically generated by an external low voltage power supply.

In one embodiment of the present invention, the negative voltage generator **120** of FIG. **4** is implemented using a charge pump circuit. FIG. **5***a* shows a simplified block diagram of one exemplary embodiment **200** of the negative voltage generator **120** of FIG. **4**. As shown in the simplified block diagram of FIG. **5***a*, the negative voltage generator includes an oscillator **202**, a clock generator circuit **204**, and an inventive charge pump circuit **206**. The oscillator **202** output is input to the clock generator circuit **204**. The output of the clock generator circuit **204** is input to the charge pump circuit **206**. The negative voltage generator **120** provides the

negative power supply voltage used by the other circuits of the fully integrated RF switch **100**.

Many prior art RF switches disadvantageously require that the negative power supply voltages be generated by circuitry that is external to the RF switch circuitry. Other RF switch implementations use a coupling approach necessary to shift the DC value of the RF input signal to the midpoint of the applied bias voltage. This approach generally requires that relatively high bias voltages be applied because of the effective halving of the FET gate drive due to this level shifting. If the bias voltages are not increased, this produces a negative effect on the switch insertion loss because the gate drive is thereby reduced and the FET channel resistances are increased.

To address these problems, one embodiment of the fully integrated RF switch **100** uses the inventive charge pump circuit **206** shown in detail in FIG. **5***b*. As shown in FIG. **5***b*, a first embodiment of the charge pump circuit **206** includes two P-channel MOSFET transistors, **208** and **210**, connected in series with two N-channel MOSFET transistors **212** and **214**. The left leg of the charge pump circuit **206** (comprising the first P-channel transistor **208** connected in series with the first N-channel transistor **212**) is coupled to the right leg of the charge pump circuit (comprising the second P-channel transistor **210** connected in series with the second N-channel transistor **214**) using a first capacitor Cp **216**. The source of the second P-channel transistor **214** is coupled to a second capacitor, an output capacitor, C **218**, as shown. Two non-overlapping clock control signals, "Clk**1**" and "Clk**2**", are used to control the operation of the transistors **208**, **210**, **212** and **214**. For example, as shown in FIG. **5***b*, the inverse of "Clk**1**", "Clk**1**_", control the gates of the P-channel transistors **208**, **210**. The other non-overlapping clock control signal, "Clk**2**", controls the gate of the N-channel transistors **212**, **214**, as shown.

The charge pump **206** generates a negative power supply voltage (−Vdd) by alternately charging and discharging the two capacitors (Cp **216** and the output capacitor C **218**) using the non-overlapping clock input signals Clk**1** and Clk**2** to drive the transistor gates. The negative power supply voltage, −Vdd, is generated from the charge that is stored on the capacitor C **218**. In one embodiment, a pulse shift circuit (not shown) is used to generate a pulse train that drives the charge pump (i.e., the pulse train is input as the clock input signals Clk**1** and Clk**2**). As the pulse train is applied to the charge pump **206**, the capacitor Cp **216** is applied the positive power supply Vdd and then discharged across the output capacitor C **218** in an opposite direction to produce the negative power supply voltage −Vdd. No transistor in the charge pump must standoff more than Vdd across any source/drain nodes, hence greatly increasing the reliability of the charge pump **206**.

In one embodiment of the inventive charge pump circuit **206**, the output C **218** has a capacitance of approximately 200 pF, and Cp **216** has a capacitance of approximately 50 pF. Those skilled in the charge pump design arts shall recognize that other capacitance values can be used without departing from the scope or spirit of the present invention.

In one embodiment, as shown in the simplified block diagram of FIG. **5***a*, the two non-overlapping clock signals are derived from an oscillator signal generated by an internal oscillator **202**. As shown in FIG. **5***a*, the oscillator **202** inputs an oscillation signal to a clock generator circuit **204**, which in turn, generates the two non-overlapping clock signals (in any convenient well known manner) that control the charge pump transistor gates. In one embodiment of the present inventive fully integrated RF switch **100**, the oscillator **202** comprises a relatively low frequency (on the order of a few MHz) oscillator. In this embodiment, the oscillator comprises a simple relaxation oscillator. However, as those skilled in the integrated circuit arts shall recognize, other types of oscillators can be used to practice the present invention without departing from its spirit or scope.

FIG. **5***c* shows the voltage amplitude of the two non-overlapping clock signals, Clk**1** and Clk**2**, varying over time. As shown in FIG. **5***c*, the two non-overlapping clock signals vary in voltage amplitude from −Vdd to +Vdd. In one embodiment, the clock signals vary from −3 VDC to +3 VDC. This arrangement improves the efficiency of the charge pump **206**.

The charge pump transistors, **208**, **210**, **212** and **214** advantageously comprise single-threshold N-channel (**212**, **214**) and P-channel (**208**, **210**) devices. Previous charge pump circuits require use of multi-threshold level devices. These previous implementations are therefore more complex in design and cost than the inventive charge pump circuit **206** of FIG. **5***b*. In one embodiment of the present charge pump **206**, the P-channel transistors **208**, **210** have widths of approximately 20 micro-meters, and lengths of approximately 0.8 micro-meters. The N-channel transistors **212**, **214** have widths of approximately 8 micro-meters, and lengths of approximately 0.8 micro-meters. Those skilled in the integrated circuit design arts shall recognize that other transistor dimensions can be used without departing from the scope or spirit of the present invention. The inventive charge pump circuit **206** is very efficient and performs well despite temperature and process variations.

Level Shifting Circuitry

Because the charge pump circuitry effectively doubles the power supply voltages that are applied to the circuit, careful attention must be paid to any potential reliability issues associated with these higher voltages. In order to implement the charge pump in a manner that increases the reliability of the transistors, level shifting circuitry is used to limit the gate-to-source, gate-to-drain, and drain-to-source voltages on the transistors to acceptable levels.

An inventive level shifting circuit **300** made in accordance with the present invention is shown in FIG. **6***a*. The level shifting circuit **300** is used to convert or shift typical or "normal" digital input signals (digital signals typically range from ground (GND) to +Vdd) such that they range from −Vdd to +Vdd. The reliability of the fully integrated RF switch transistors is thereby increased. In one embodiment of the present invention, the control signals are shifted to −3 VDC to +3 VDC, although those skilled in the RF switch control arts shall recognize that other level shifting voltage ranges can be used without departing from the spirit or scope of the present invention.

As shown in FIG. **6***a*, the inventive level shifting circuit **300**, hereinafter referred to as the level shifter **300**, comprises a plurality of inverters coupled in a feedback configuration. More specifically, in the embodiment shown in FIG. **6***a*, the level shifter **300** includes two groups of inverters used to generate first and second shifted output signals, "out" on a first output node **314**, and its inverse "out_" on a second output node **316**. The first group of inverters comprises inverters **302**, **304** and **306**. A second group of inverters comprises inverters **308**, **310** and **312**. A typical or "normal" digital input signal (i.e., a digital input signal that ranges from GND to +Vdd) is input to the level shifter **300** at an input node **318** of a first inverter **320**. The first inverter **320** generates a first input signal "in" (on an output node **324**) which is input to a second inverter **322**.

The second inverter **322** generates a second input signal "in_", the inverse of the first input signal "in", on an output node **326**. Therefore, **10** the first and second inverters, **320**, **322**, generate the signals that are input to the two groups of inverters described above. For example, the first input signal "in" is coupled to the input **328** of the inverter **302**. Similarly, the second input signal "in_" is coupled to the input **330** of the inverter **308**.

The output of the first group of inverters, "out", is generated by a first output inverter **306**, and is provided on a first output node **314**. The output of the second group of inverters, "out_", is generated by a second output inverter **312**, and is provided on a second output node **316**. The two level shifter outputs, "out" and "out_", are input to other circuits of the fully integrated RF switch **100** of FIG. **4**. For example, in one embodiment, the first output, "out", is coupled to the gates of the devices of the switching transistor grouping **33** and the shunting transistor grouping **38** (i.e., the "out" signal on the first output node **314** of FIG. **6***a* is coupled to the "SW" control input signal of FIG. **3**, at the input nodes **33'** and **38'**, and thereby controls the operation of the switching transistor grouping **33** and the shunting transistor grouping **38** as described above with reference to FIG. **3**). Similarly, in this embodiment, the second level shifter output, "out_", is coupled to the "SW_" control input signal of FIG. **3** (at the input nodes **34'** and **37'**) and thereby controls the switching transistor grouping **34** and the shunting transistor grouping **37** as described above.

The level shifter **300** of FIG. **6***a* shifts the DC level of an input signal (i.e., the input signal provided on the input node **318**) while leaving the frequency response of the input signal unchanged. The level shifter **300** takes full advantage of the floating technology offered by the silicon-on-insulator substrate implementation of the fully integrated RF switch **100**. The inverters of the level shifter **300** operate on a differential basis, i.e., the level shifter shifts the digital input signals based upon the difference between two voltage signals. More specifically, as long as the difference between the power supply signals provided to the inverters (such as, for example, the output inverters **306** and **312**) is on the order of Vdd, the level shifter **300** reliably functions to shift the input signals to a range between −Vdd to +Vdd. In one embodiment, Vdd is equal to 3 VDC. In this embodiment, the transistors comprising the inverters of the level shifter **300** (e.g., the output inverters **306** and **312**) never have greater than 3 VDC applied across their source/drain nodes. This increases the reliability of the transistor devices.

Referring again to FIG. **6***a*, the level shifter uses a feedback approach to shift the digital input signals to voltage levels ranging from −Vdd to +Vdd. Specifically, the output of the second group of inverters (**308**, **310**, **312**) on the second output node **316** (i.e., the "out_" signal) is provided as feedback to an input of the first group of inverters at the input of the inverter **304**. Similarly, the output of the first group of inverters (**302**, **304**, **306**) on the first output node **314** (i.e., the "out" output signal) is provided as input to the second group of inverters, specifically, is provided as input to the inverter **310**.

When the digital input signal on the input node **318** reaches a logical "high" state (i.e., in some embodiments, when the input signal transitions from GND to +Vdd), the "in" signal (at the node **324**) and the "in_" signal (at the node **326**) go to ground (e.g., 0 VDC) and Vdd (e.g., 3 VDC), respectively. The "out" signal at the first output node **314** is driven to +Vdd. At the same time, the "out_" signal at the second output node **316** is driven towards −Vdd. The feedback (of "out_" fed back to the input of the inverter **304** and "out" fed forward to the input of the inverter **310**) configuration ensures the rapid change in state of the level shifter **300**. The level shifter **300** works similarly when the input signal transitions from a logic high to a logic low state (i.e., transitions from +Vdd to GND). When the digital input signal on the input node **318** reaches a logic "low" state, the "in" signal (at the node **324**) and the "in_" signal (at the node **326**) go to Vdd (e.g., 3 VDC), and ground, respectively. The "out" signal at the first output node **314** is driven to −Vdd. At the same time, the "out_" signal at the second output node **316** is driven towards +Vdd. The feedback again ensures the rapid change in state of the level shifter **300**. The grounding contribution ensures that the level shifter inverters never see more than a full Vdd voltage drop across the source/drain nodes of the MOSFET transistors of the inverters.

FIG. **6***b* shows one embodiment of the inverters (e.g., the inverters **302**, **304**, and **306**) used to implement the level shifter **300** of FIG. **6***a*. As shown in FIG. **6***b*, the inverter **340** includes two MOSFET devices, a P-channel transistor **342** and an N-channel transistor **344**. The devices are connected in series as shown, having their gates coupled together and controlled by an input signal provided at an input node **346**. The source of the P-channel transistor **342** is coupled to a first power supply voltage signal at node **350**, while the source of the N-channel transistor **344** is coupled to a second power supply voltage signal at a node **352**. The device drains are coupled together as shown to produce an output of the inverter at an output node **348**. In one embodiment of the present inventive inverter **340**, the P-channel transistor **342** has a width of 5 micro-meters and a length of 0.8 micro-meters. In this embodiment, the N-channel transistor has a width of 2 micro-meters and a length of 0.8 micro-meters. Those skilled in the transistor design arts shall recognize that other physical dimensions can be used for the transistors of the inverter **340** without departing from the scope or spirit of the present invention. A logical representation of the inverter **340** is also shown as symbol **360** in FIG. **6***b*.

Thus, using the present inventive level shifter **300**, digital input signals that initially range from GND to +Vdd are shifted to range from −VDD to +Vdd. FIG. **7***a* shows a voltage amplitude versus time plot of the digital input signal and the corresponding output signal that is generated by the inventive level shifter **300** of FIG. **6***a*. As shown in FIG. **7***a*, the digital input signal ranges from ground, or 0 VDC to Vdd. The output of the inventive level shifter **300** ranges from −VDD to +Vdd. In one embodiment of the present inventive RF switch, the input signal ranges from 0 VDC to +3 VDC, and the output of the level shifter **300** ranges from −3 VDC to +3 VDC. Other values of power supply voltages can be used without departing from the scope or spirit of the present invention. For example, in one embodiment, the input signal can range from 0 to +3.5 VDC, or from 0 to 4 VDC. In this embodiment, the level shifter shifts the signal to range from −3.5 (or −4) VDC, to +3.5 (or +4) VDC.

FIG. **7***b* shows a simplified logic symbol for the inventive level shifter **300** of FIG. **6***a*. This logic symbol is used in subsequent figures. As shown in FIG. **7***b*, the digital input signal is provided on the input node **318** (the same input node **318** described above with reference to FIG. **6***a*). The level shifter **300** provides two shifted outputs, "out" and its inverse "out_", and these are provided on output nodes **314** and **316**, respectively (the same output nodes **314**, **316** described above with reference to FIG. **6***a*).

RF Buffer Circuit

FIG. **8***a* is an electrical schematic of a two-stage level shifter and RF buffer circuit **400**.

FIG. **8***b* is a simplified block diagram of the digital control input and interface to the RF buffer circuit **400**. The two-stage level shifter and RF buffer circuit **400** of FIG. **8***a* comprises a first stage level shifter **300** and a second stage RF buffer circuit **402**. The first stage level shifter **300** is identical to that described above with reference to FIGS. **6***a*, **6***b*, **7***a* and **7***b*, and is therefore not described in more detail here. As described above, the level shifter stage **300** shifts the logic levels of the digital control signals to range from −VDD and +Vdd. The second stage of the circuit **400** comprises the RF buffer circuit **402**. The RF buffer circuit **402** acts as a driver stage only (i.e., no level shifting is performed by the RF buffer circuit).

The RF buffer electrically isolates the digital control signals (such as those generated by the CMOS logic block **110** of FIG. **4**) from the RF switch **30** described above with reference to FIG. **3**. The RF buffer **402** functions to inhibit drooping of the control voltages (SW, SW_, which are also referred to herein and shown in FIG. **8***a*as the control signals "out" and "out_, respectively) that control the enabling and disabling of the transistors in the RF switch **30**. As described below in more detail, the RF buffer **402** also functions to prevent coupling of large power RF signals to the negative power supply (i.e., −VDD) that is generated by the charge pump circuit **206** described above with reference to FIGS. **5***a*-**5***c*. More specifically, the RF buffer **402** prevents large power RF signals extent in the RF switch **30** from RF-coupling to, and thereby draining current from, the negative power supply generated by the charge pump **206** (FIG. **5***b*).

When very large power RF input signals are input to the inventive RF switch **30**, coupling of the RF signals to the digital logic signals can occur unless an RF buffer circuit is used to isolate the digital logic signals from the RF switch. The RF coupling can and usually will detrimentally affect the RF transistor control signals (SW and SW_). For example, when RF input signals on the order of approximately 30 dBm are input to a 1 watt RF switch **30**, RF coupling can cause voltage swings of several tenths of a volt on the digital control lines. This is due to the feedback of RF signals from the RF switch through to the digital control circuitry. This RF coupling effect can adversely affect the enabling and disabling of the RF transistor groupings and hence the proper operation of the RF switch **30**. The buffer circuit **402** of FIG. **8***a* prevents the undesirable RF coupling effect.

As shown in FIG. **8***a*, the inventive buffer circuit **402** is very similar in configuration to the level shifter **300** described above and shown as the first stage of the two-stage circuit **400**. Similar to the level shifter **300**, the RF buffer **402** comprises two groups of inverters, a first group of inverters (**404**, **406** and **408**) and a second group of inverters (**410**, **412**, and **414**). The output of the first group of inverters (**404**, **406**, and **408**), generated by the first output inverter **408**, is labeled "out" in the figure and is provided at a first output node **416**. The output of the second group of inverters (**410**, **412**, and **414**), generated by the second output inverter **414**, is labeled "out_", and is provided at a second output node **418**. The output signal "out_" is the inverse of the output signal "out".

Importantly, although the first stage level shifter **300** uses feedback to perform the level shifting function (as described above with reference to FIG. **6***a*), the RF buffer circuit **402** does not feedback its output signals to the input. Consequently, the digital input signals input to the first stage (i.e., the control input signals that are input to the level shifter **300** at the nodes **328** and **330**) are isolated from the output signals that are used to control the RF switch transistors (i.e., the control output signals "out" and its inverse signal "out_" at the output nodes **416** and **418**, respectively, and coupled to the SW and SW_ control signal lines, respectively).

More specifically, and referring again to FIG. **8***a*, the level shifter **300** inputs the digital control signals "in" and its inverse signal "in_" at the nodes **328**, **330** respectively (as described in more detail above with reference to FIG. **6***a*). The first output of the level shifter **300**, "out**1**", at the output node **314**, is fed back to the input of the inverter **310** as shown. Similarly, the second output of the level shifter **300**, "out**1**_", at the output node **316**, is fed back to the input of the inverter **304**. As described above, because of this feedback topology, RF coupling occurs (i.e., the level shifter output signals have RF signals superimposed thereon) if the output signals of the level shifter are used to directly control the RF switch transistors (i.e., in the absence of the buffer circuit **402**). Therefore the inventive RF buffer circuit **402** is used without feedback of the output signals to isolate the input signals (i.e., the digital input signals "in" and "in_) from the RF signals present in the RF switch. As shown in FIG. **8***a*, the first output signal "out**1**" of the level shifter **300** is input to the inverters **404**, **406** of the RF buffer circuit. Similarly, the second output signal "out**1**_" of the level shifter **300** is input to the inverters **410**, **412** of the buffer circuit. The two control outputs of the RF buffer circuit **402** ("out" and "out_") control the enabling and disabling of the transistors of the RF switch and are not provided as feedback to the level shifter. Hence, improved isolation between the RF switch and the digital logic circuitry is achieved.

In one embodiment, the inverters used to implement the two-stage level shifter and RF buffer circuit **400** comprise the inverter **340** described above with reference to FIG. **6***b*. However, those skilled in the inverter design arts shall recognize that alternative inverter designs can be used in implementing the two-stage circuit **400** without departing from the scope or spirit of the present invention. In one embodiment, the transistors used to implement the first stage level shifter **300** are physically smaller than those used to implement the second stage RF buffer circuit **402**. Larger dimension transistors are used in the RF buffer circuit **402** to achieve an efficient amplification of the control signals. For example, in one embodiment, the transistors used to implement the RF buffer are three times wider than those used to implement the level shifter **300**, resulting in an amplification of approximately three times the current. Those skilled in the transistor design arts shall recognize that other convenient transistor dimensions can be used to achieve any desired amplification of the digital control signals.

Voltage Divider for Use in an Alternative Level Shifting Circuit of the Present Invention

FIG. **9***a* is an electrical schematic of one embodiment of a low current voltage divider ("LCVD") circuit **500** that is used in the feedback path of one embodiment of the level shifter **300** described above with reference to FIG. **6***a*. FIG. **9***b* shows a simplified logic symbol that is used to represent the voltage divider **500** of FIG. **9***a*. The voltage divider **500** is used in one embodiment to address potential gate oxide reliability issues related to excessive voltage swings across the gate oxides of the feedback inverter transistors. As described above with reference to the level shifter **300**, although the source-to-drain voltages of the various MOSFETs used to implement the level shifter are never applied voltages greater than Vdd, because the outputs of the level shifter (i.e., the output signals "out" and "out_) can swing as much as 2*Vdd (i.e., from −VDD to +Vdd), the gate oxides of the feedback inverters **304** and **310** can have applied

voltages of 2*Vdd. These feedback voltage levels can be applied across the gate oxides of the feedback inverters **304**, **310**, and can result in gate oxide reliability problems.

The gate oxide reliability issues can be averted by ensuring that the maximum voltage applied across the gate oxide of the feedback inverters **304**, **310** is lowered to approximately Vdd (as contrasted with gate oxide voltages of 2*Vdd). Therefore, in one embodiment of the present inventive fully integrated RF switch, the voltage divider of FIG. **9***a* limits the voltages applied to the gates of the level shifter feedback inverters **304**, **310**. In this embodiment, instead of directly feeding back the level shifter outputs to their respective feedback inverters as shown in the level shifter of FIG. **6***a* (i.e., the outputs "out" and "out_", at the output nodes **314**, **316**, respectively), the level shifter output signals are first conditioned by the voltage divider **500** of FIG. **9***a* before being fed back to the feedback inverters. As described below in more detail, the voltage divider **500** ensures that the voltages applied to the gate oxides of the feedback inverters **304**, **310** do not exceed more than approximately Vdd plus a small voltage drop (the voltage drop being a function of the number of transistors used to implement the voltage divider **500** and a transistor threshold voltage). In one embodiment Vdd is 3 VDC, and the voltage drop is 0.9 VDC. In this embodiment, the voltage divider **500** ensures that the gate oxides are never applied voltages exceeding approximately 3.9 VDC (i.e., the feedback inverters are applied voltages that range from −3 VDC to 0.9 VDC).

Referring now to FIG. **9***a*, the voltage divider **500** includes a plurality of MOSFET devices (**502**, **504**, **506** and **508**) coupled together in a serial configuration (i.e., stacked on top of each other in a source to drain arrangement as shown). In one embodiment, the gate and drain of the MOSFETs **502**, **504**, **506** and **508** are coupled together to implement stacked diodes. The diode-implementing MOSFETs, hereafter referred to as "diode devices", are stacked in series as shown. The voltage divider **500** also includes a MOSFET M3 **510** and an output MOSFET M2 **512**. The function of these two transistors is described in more detail below.

The diode devices are used to divide the voltage of an input signal provided to the voltage divider **500** at an input node **514**. As shown in FIG. **9***a*, the signal that is divided by the voltage divider **500** is provided as input to the drain (and connected gate) of the first device **502**. Once the input signal exceeds a positive voltage level of (n*Vthn), where "n" is the number of diode devices used to implement the voltage divider **500**, and Vthn is the threshold voltage of the device (i.e., the "diode-drop" from the drain to the source of the device), the diode devices (**502**, **504**, **506**, and **508**) begin to conduct current heavily. In the embodiment shown in FIG. **9***a*, n=4, and Vthn =0.7 volts, although alternative values for "n" and Vthn **30** can be used without departing from the scope or spirit of the present invention. For example, in other embodiments, the input signal provided to the divider can be limited to any desired voltage level by varying the number of diode devices used to implement the voltage divider **500** (i.e., by varying the value of "n"). In the embodiment shown in FIG. **9***a*, once the input voltage exceeds a voltage level of (4*0.7), or 2.8 volts, the stacked diode devices begin conducting heavily.

A ballast resistor, R **516**, is connected to the source of the output diode device **508** as shown. Once the diode devices turn on fully, the ballast resistor R **516** drops any additional input voltage that exceeds the value of n*Vthn. In the embodiment shown in FIG. **9***a*, the ballast resistor R **516** drops any additional input voltage exceeding the value of (input voltage−(4*Vthn)). The output of the voltage divider **500** is tapped from the connected gate-drain of the output diode device **508**. The voltage-divided output signal is provided on an output node **520**. Due to the diode voltage drops of the diode devices **502**, **504**, **506**, (i.e., 3*Vthn), and the voltage dropped across the ballast resistor R **516**, the output at the output node **520** is guaranteed to never exceed approximately (input voltage−(3*Vthn)). For Vthn=approximately 0.7 volts, and a maximum input voltage of approximately 3 volts, the output node **520** will never exceed (3 VDC−(3*0.7 VDC)), or 0.9 VDC. Thus, in the embodiment shown in FIG. **9***a*, for an input voltage ranging between −3 VDC to +3 VDC, the voltage divider **500** limits the output of the output node **520** to a range of −3 VDC to 0.9 VDC.

The output MOSFET M2 **512** is configured as a capacitor and is used to assist in accelerating the switching time of the voltage divider **500**. The MOSFET M3 **510** assures that the output node **520** swings to the potential of the input signal at the input node **514** when the input goes to a negative potential. This is accomplished by the device M3 **510** turning on when the input signal goes to a negative potential. Thus, when the input signal goes to a −VDD potential (e.g., −3 VDC), the output signal at the output node **520** also goes to −VDD. The output device **508** is reversed biased during negative voltage swings of the input signal assuring that no DC current is drained from the negative power supply during the negative voltage swings of the input signal. When the voltage divider output is approximately −3 VDC, the voltage divider **500** draws no current. This is important because a current at −3 VDC discharges the charge pump circuit described above with reference to FIG. **5***b*. When the voltage divider output is approximately 0.9 volts, the current that is drawn is very small if the ballast resistor R **516** is selected to be relatively large. However, because the current in this case occurs between a positive voltage (0.9 volts) and ground, no additional charge pump current is delivered due to the operation of the voltage divider **500** of FIG. **9***a*.

In one embodiment, the ballast resistor R **516** has a value of 100 k-ohms. In one embodiment all of the devices of the voltage divider **500** have the same length. For example, in one embodiment, all of the devices have a length of 0.8 micro-meters. In one embodiment, all of the diode devices (**502**, **504**, **506**, and **508**) have identical physical dimensions. In one embodiment, the diode devices each have a width of 2 micro-meters, the device M3 **510** has the same width of 2 micro-meters, and the output MOSFET M2 **512** has a width of 14 micro-meters. Those skilled in the integrated circuit design arts shall recognize that other values and alternative configurations for the devices shown in FIG. **9***a* can be used without departing from the scope or spirit of the present invention. For example, those skilled in the electrical circuit design arts shall recognize that other voltage divider output levels can easily be accommodated by varying the number "n" of diode elements, varying the values of Vthn, or by tapping the output node **520** at a different point in the stack of diode devices (e.g., by tapping the output from the drain of diode device **506**, or **504**, instead of from the drain of device **508** as shown).

Modified Level Shifter using the Voltage Divider

By reducing the voltages that are applied to the gate oxides of the RF switch transistors, the voltage divider **500** of FIGS. **9***a* and **9***b* advantageously can be used to increase the reliability of the transistors in both the level shifter **300** and the charge pump circuit described above. For example, FIG. **10** shows a modified level shifter **600** using the voltage

divider **500** of FIG. **9***a* in combination with the level shifter **300** of FIG. **6***a*. As shown in FIG. **10**, the output (at output node **314**) of the inverter **306** of the level shifter **300** is applied to an input of a first voltage divider **500'**. Similarly, the output (at the output node **316**) of the inverter **312** of the level shifter **300** is applied to an input of a second voltage divider **500"**. The outputs of the voltage dividers are fed back to the input of the feedback inverters **304**, **310** as shown in FIG. **10**. Specifically, and referring to FIG. **10**, the output of the first voltage divider, "out", on the output node **520'** is fed back to the input of the feedback inverter **310**. Similarly, the output of the second voltage divider, "out_", on the output node **520"** is fed back to the input of the feedback inverter **304**. As described above with reference to FIG. **9***a*, the level shifters **500'** and **500"** reduce the feedback voltages to ranges of −VDD to approximately +0.9 VDC. This reduced voltage swing on the feedback paths does not alter the function of the level shifter **600**.

Note that the RF switch control signals, "SW" and "SW_", can be tapped from the level shifter outputs prior to their input to the voltage dividers **500'** and **500"**, and provided as input to the inventive RF switch **30** of FIG. **3**. For example, as shown in FIG. **10**, the output of inverter **306** at the output node **314** can be tapped and used to generate the switch control signal "SW". Similarly, the output of the inverter **312** at the output node **316** can be tapped and used to generate the switch control signal "SW_". In one embodiment, as described above with reference to the two-stage level shifter and RF buffer circuit **400** of FIG. **8***a*, the control signals tapped from the nodes **314**, **316** are first buffered before being coupled to the RF switch transistors. The switch control signals, SW and SW_, are allowed to have a full-rail voltage swing which does not create gate oxide reliability problems in the RF switch. More specifically, the switch control signals range from −VDD to +Vdd (i.e., the voltage levels of the switch control signals are not limited by the voltage dividers). The full voltage swings of the switch control signals do not raise gate oxide reliability issues with respect to the RF switch MOSFETs because the sources of the RF switch MOSFETs are grounded. The switch input signals are therefore relative to ground in the RF switch MOSFETs. Consequently, the MOSFETs are applied either a positive Vdd voltage relative to ground across the gate oxides, or a negative Vdd voltage relative to ground across the gate oxides.

FIG. **10** also shows a simplified symbolic representation **601** of a section of the modified level shifter **600**. The symbol **601** represents the portion indicated by the dashed region **601'** of FIG. **10**. As shown in FIG. **10**, the symbolic modified level shifter **601** includes a first input "in_" **630** corresponding to the input node **326** ("in_"). The symbolic level shifter **601** also includes a second input "out" **632** corresponding to the input to the feedback inverter **310**. Note that this signal is also derived from the output **520'** of the first voltage divider **500'**. A positive power supply voltage is input at a +Vdd input **634**. A negative power supply voltage is input at a −VDD input **636**. The modified level shifter **601** has three output signals, "out_pos" (at output **638**), "out_neg" (at output **640**), and "out_" (at output **642**). These outputs correspond to the output nodes **606**, **608**, and **520"** described above. For ease of understanding, the symbolic representation of the level shifter **601** is used in the figures described below.

The potential gate oxide reliability problems associated with the level shifter **300** described above with reference to FIG. **6***a* are averted using the voltage dividers **500'** and **500"** in the feedback paths of the modified level shifter **600**. In addition, the voltage dividers **500'** and **500"** can also function to reduce potential gate oxide reliability problems associated with the charge pump circuit. As shown in FIG. **10**, the outputs of the inverters **308** and **310** are tapped from the level shifter **300** and provided as input to two output inverters to produce two output signals, "out_pos" and "out_neg." More specifically, the output of the inverter **308** is provided as input to a first output inverter **602**. Similarly, the output of the feedback inverter **310** is provided as input to a second output inverter **604**.

By coupling the output inverters **602**, **604** in this manner, the modified level shifter **600** output signals never exceed Vdd (or −VDD). More specifically, the first output inverter **602** generates an output signal, "out_pos", at a first output node **606**, that ranges from GND (i.e., 0 VDC) to +Vdd. The second output inverter **604** generates a second output signal, "out_neg", at a second output node **608**, that ranges from −VDD to GND. When the input signal "in_" goes to GND, the output signal "out_pos" also goes to GND. The output signal "out_neg" transfers from GND to −VDD. When the input signal "in_" goes positive to +Vdd, "out_pos" also goes to Vdd, and "out_neg" transfers from −VDD to GND. Thus, using the present modified level shifter **600**, the "out_pos" output signal ranges from GND to +Vdd, while the "out_neg" output signal ranges from −VDD to GND. As described below in more detail, the two output signals, "out_pos" and "out_neg", are used to address potential gate oxide reliability problems in a modified charge pump circuit. As described now with reference to FIGS. **11***a* and **11***b*, these output signals can also be used to address potential gate oxide reliability problems in the RF buffer circuit.

Modified Level Shifter and RF Buffer Circuit

The two-stage level shifter and RF buffer **400** described above with reference to FIG. **8***a* can experience voltage swings at the RF buffer inverter inputs of approximately 2*Vdd. As already described, this level of voltage swing may present gate oxide reliability problems and detrimentally affect the function of the RF buffer transistors.

FIGS. **11***a* and **11***b* show an alternative embodiment **400'** of the two-stage level shifter and RF buffer circuit **400** described above with reference to FIG. **8***a*. The alternative embodiment of the RF buffer shown in FIG. **11***b* uses the voltage divider circuit described above to assure that voltages on the gate oxides of the RF buffer never exceed greater than 0.9 volts above Vdd. As shown in FIG. **11***b*, the alternative two-stage level shifter and RF buffer circuit **400'** includes a first stage level shifter circuit **600** coupled to a second stage RF buffer circuit **402'**. In this embodiment of the level shifter and RF buffer circuit **400'**, the modified level shifter outputs, "out_pos" and "out_neg", described above with reference to FIG. **10**, are used as input to the RF buffer inverters to generate the RF buffer output signals "out" and "out_". For example, as shown in FIG. **11***b*, the "out_pos" and "out neg" output signals generated by a first modified level shifter **700** are input to two RF buffer inverters, **702**, **704**, respectively. Similarly, the "out_pos" and "out_neg" output signals generated by a second modified level shifter **706** are input to two RF buffer inverters, **708**, **710**, respectively. In accordance with the alternative embodiment **400'** shown in FIGS. **11***a* and **11***b*, when an input signal "in" is a logical high signal, the "out_pos" output goes to Vdd while the "out_neg" goes to GND. Thus, when the input signal "in" is a logical high value, the output of the inverter **702** goes to GND, and the output of the inverter **704** goes to −Vdd. Therefore, when the input signal "in" is high, the

output of the inverter **712** ("out") goes to −VDD. When the input signal "in" is low, the opposite outputs are produced.

The RF buffer inverters **702**, **704** are used to control the power supply voltages of a first RF output inverter **712**. Similarly, the RF buffer inverters **708**, **710** are used to control the power supply voltages of a second RF output inverter **714**. In this embodiment, the RF buffer output signals, "out" and "out_", are used to control the RF switch (i.e., output signal "out" acts as control voltage "SW", while "out_" acts as control voltage "SW_").

Modified Charge Pump—An Alternative Embodiment

As noted above, the two output signals "out_pos" and "out_neg" generated by the modified level shifter **600** of FIG. **10** can be used in an alternative embodiment of the charge pump circuit to reduce or eliminate potential gate oxide reliability problems associated with excessive voltages applied to the charge pump. As described above with reference to FIGS. **5***b* and **5***c*, the clock signals used to control the gates of the charge pump transistors (i.e., the P-channel transistors **208**, **210**, and the N-channel transistors **212**, **214**) have voltage swings of 2 *Vdd. For example, as shown in FIG. **5***c*, the charge pump clock signals, "Clk**1**" and "Clk**2**", range from the negative power supply voltage −VDD to the positive power supply voltage +Vdd. Similar to the gate oxide reliability issues described above with reference to the RF buffer and level shifter circuits, this full-rail voltage swing may present oxide reliability problems in the charge pump circuit. Therefore, a modified charge pump circuit is shown in FIG. **12** which reduces or eliminates potential gate oxide reliability problems by limiting the voltages applied to gate oxides to range from −VDD to 0.9 volts.

FIG. **12** shows a modified charge pump **800** that uses the modified level shifter **600** described above with reference to FIG. **10**. As shown in FIG. **12**, the modified charge pump **800** comprises a charge pump circuit **206'** and an inventive charge pump clock generation circuit **802**. The charge pump clock generation circuit **802** generates the clock control signals used by the charge pump circuit **206'**. The charge pump circuit **206'** is very similar in design to the charge pump **206** described above with reference to FIG. **5***b*. For example, the charge pump **206'** includes a pair of P-channel transistors **208**, **210**, and a pair of N-channel transistors **212**, **214**, in addition to a pass capacitor Cp **216** and an output capacitor C **218**. In one embodiment of the charge pump circuit **206'**, the output capacitor C **218** has a capacitance on the order of a few hundred pF, and the capacitor Cp **216** has a capacitance of approximately 50 pF. Those skilled in the charge pump design arts shall recognize that other capacitance values can be used without departing from the scope or spirit of the present invention.

The charge pump **206'** functions very similarly to the charge pump **206** described above with reference to FIG. **5***a*, and therefore its operation is not described in detail again here. The charge pump **206'** shown in FIG. **12** differs from the charge pump **206** in that the control signals used to control the charge pump **206'** transistor gates (i.e., the gates of the transistors **208**, **210**, **212**, and **214**) are limited to half-rail voltage swings (i.e., they are limited to range from −VDD to ground, or from ground to Vdd). Potential gate oxide reliability problems invoked when the gate control voltages are allowed to swing a full rail (i.e., from −VDD to Vdd) are thereby reduced or eliminated.

As shown in FIG. **12**, the charge pump clock generation circuit **802** includes four modified level shifters **804**, **806**, **808** and **810**, coupled together in a feedback configuration. In one embodiment of the modified charge pump, the four modified level shifters are implemented by the modified level shifter **600** described above with reference to FIG. **10**. FIG. **12** shows the level shifters using the symbolic representation **601** of the level shifter **600** of FIG. **10**. In this embodiment, the level shifters **804**, **806**, **808**, and **810** perform identically to the level shifter **600** of FIG. **10**. The two non-overlapping clock signals, "Clk**1**", and "Clk**2**" (and their inverse signals, "Clk**1**_" and "Clk**2**_", respectively) are input to the "in_" inputs of the level shifters as shown in FIG. **12**. The two input clock signals, "Clk**1**" and "Clk**2**", are identical to the non-overlapping clock signals described above with reference to FIGS. **5***a*–**5***c*. As shown above with reference to FIG. **5***c*, the two non-overlapping clock signals vary in voltage amplitude from −VDD to +Vdd. In one embodiment, the clock signals vary from −3 VDC to +3 VDC.

The four modified level shifters generate the half-rail clock control signals that are used to control the charge pump **206'**. Specifically, as shown in FIG. **12**, the four level shifters generate the "CLK**1**POS_", "CLK**1**NEG_", "CLK**2**POS", and "CLK**2**NEG" control signals that are input to the charge pump transistor gate control nodes **250**, **252**, **254** and **256**, respectively. In the embodiment shown in FIG. **12**, the level shifters **806** and **808** generate the four transistor gate control signals "CLK**1**POS_", "CLK**1**NEG_", "CLK**2**POS", and "CLK**2**NEG". The level shifter **806** generates the "CLK**1**POS_" and "CLK**1**NEG_" gate control signals, while the level shifter **808** generates the "CLK**2**POS", and "CLK**2**NEG" gate control signals. More specifically, as shown in FIG. **12**, the "out_pos" output of the level shifter **806** ("CLK**1**POS_") is coupled to control the transistor gate input **250** of the transistor **208**. The "out_neg" output of the level shifter **806** ("CLK**1**NEG_") is coupled to control the transistor gate input **252** of the transistor **210**. Similarly, the "out_pos" output of the level shifter **808** ("CLK**2**POS") is coupled to control the transistor gate input **254** of the transistor **214**. Finally, the "out_neg" output of the level shifter **808** ("CLK**2**NEG") is coupled to control the transistor gate input **256** of the transistor **214**. The clock generation circuit **802** functions to prevent excessive voltages across the gate oxides of the charge pump transistors.

Those skilled in the transistor design arts shall recognize that other control configurations can be used without departing from the spirit or scope of the present invention. For example, the other two level shifters (**804**, **810**) can be used to generate the control signals in an alternative embodiment of the modified charge pump. Also, as described above with reference to the charge pump circuit **206**, alternative transistor configurations (N-channel and P-channel) can be used to implement the modified charge pump **206'** of the present invention.

As shown in FIG. **12**, the four level shifters **804**, **806**, **808** and **810** are coupled together in level shifter pairs (**804** with **806**, and **808** with **810**) in a feedback configuration that is very similar to the feedback topology of the level shifter described above with reference to FIG. **6***a*. For example, the "out_" output node of the level shifter **804** is provided as feedback to the "out" node of its associated pair level shifter **806**. Similarly, the "out_" output node of the level shifter **806** is provided as feedback to the "out" node of its associated pair level shifter **804**. Similarly, the "out_" output node of the level shifter **808** is provided as feedback to the "out" node of its associated pair level shifter **810**. The "out_" output node of the level shifter **810** is provided as feedback to the "out" node of its associated pair level shifter **808**. The feedback configuration is used by the clock generation

circuit **802** in the generation of the four transistor gate control signals "CLK1POS_", "CLK1NEG_", "CLK2POS", and "CLK2NEG".

Summary

A novel RF switch is provided wherein the switch is fabricated using an SOI CMOS process. Fabricating the switch on an SOI substrate results in lack of substrate bias and allows the integration of key CMOS circuit building blocks with the RF switch elements. Integration of the CMOS building blocks with RF switch elements provides a fully integrated RF switch solution that requires use of only a single external power supply (i.e., the negative power supply voltage is generated internally by a charge pump circuit integrated with the RF switch). This results in improvements in RF switch isolation, insertion loss and compression. In one embodiment, the RF switch has a 1 dB compression point exceeding approximately 1 Watt, an insertion loss of less than approximately 0.5 dB, and switch isolation as high as approximately 40 dB. The inventive switch also provides improvements in switching times.

A number of embodiments of the present invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention.

Accordingly, it is to be understood that the invention is not to be limited by the specific illustrated embodiments, but only by the scope of the appended claims.

What is claimed is:

1. An RF switch circuit for switching RF signals, comprising:

(a) a first input port receiving a first RF input signal;

(b) a second input port receiving a second RF input signal;

(c) an RF common port;

(d) a first switch transistor grouping comprising a plurality of FETs arranged in a stacked configuration, wherein each of said FETs has a gate that is insulated from its channel, wherein said first switch transistor grouping has a first node coupled to the first input port and a second node coupled to the RF common port, and wherein the first switch transistor grouping is controlled by a switch control signal (SW);

(e) a second switch transistor grouping comprising a plurality of FETs arranged in a stacked configuration, wherein each of said FETs has a gate that is insulated from its channel, wherein said second transistor grouping has a first node coupled to the second input port and a second node coupled to the RF common port, and wherein the second switch transistor grouping is controlled by an inverse (SW_) of the switch control signal (SW);

(f) a first shunt transistor grouping comprising a plurality of FETs arranged in a stacked configuration, wherein each of said FETs has a gate that is insulated from its channel, wherein said first shunt transistor grouping has a first node coupled to the second input port and a second node coupled to ground, and wherein the first shunt transistor grouping is controlled by the switch control signal (SW); and

(g) a second shunt transistor grouping comprising a plurality of FETs arranged in a stacked configuration, wherein each of said FETs has a gate that is insulated from its channel, wherein said second shunt transistor grouping has a first node coupled to the first input port and a second node coupled to ground, wherein the second shunt transistor grouping is controlled by the inverse (SW_) of the switch control signal (SW);

wherein, when SW is enabled, the first switch and shunt transistor groupings are enabled while the second switch and shunt transistor groupings are disabled, thereby passing the first RF input signal through to the RF common port and shunting the second RF input signal to ground; and wherein when SW is disabled, the second switch and shunt transistor groupings are enabled while the first switch and shunt transistor groupings are disabled, thereby passing the second RF input signal through to the RF common port and shunting the first RF input signal to ground.

2. The RF switch circuit of claim **1**, wherein the switch circuit is fabricated in a silicon-on-insulator (S0I) technology.

3. The RF switch circuit of claim **1**, wherein the switch circuit is fabricated on an Ultra-Thin-Silicon ("UTSi") substrate.

4. The RF switch circuit of claim **3**, wherein the FETs are MOSFET transistors formed in a thin silicon layer on a fully insulating sapphire wafer.

5. The RF switch circuit of claim **1**, intended for switching RF signals having an operating period 1/Fo, wherein the gate of each FET has a capacitance Cg to its channel, and the gate is coupled to a control voltage via a gate resistor Rg having a value such that Rg*Cg>1/Fo.

6. The RF switch circuit of claim **1**, wherein the gate of each FET is coupled to a control voltage via a gate resistor Rg having a value of at least about 30 kΩ.

7. The RF switch circuit of claim **2**, wherein the circuit is designed for switching RF signals at an operating frequency Fo, the FETs are MOSFETs, the gate of each FET has a capacitance Cg to its channel, and the gate is coupled to a control voltage via a gate resistor Rg having a value such that Rg*Cg>1/Fo.

8. The RF switch circuit of claim **7**, wherein the stacked MOSFETs of each grouping of transistors share the signal voltage substantially equally without a need for ballast resistors parallel to a conduction path of such stacked MOSFETs, and wherein all Rg of the MOSFETs of each particular grouping are commonly controlled by a corresponding switching voltage.

9. The RF switch circuit of claim **8**, wherein the gate resistors coupled to the transistor gate nodes of the second switch and shunt transistor groupings are commonly coupled to the inverse switch control signal SW_.

10. The RF switch circuit of claim **1**, wherein the FETs are MOSFETs having associated gate capacitance and an associated gate resistor coupling the gate to a drive signal, wherein RC time constants associated with each MOSFET within the transistor groupings are functions of the associated gate resistors and the associated gate capacitances, and wherein the RC time constant of each transistor far exceeds a period of the RF input signals thereby causing RF voltages to be shared equally across the MOSFETs.

11. The RF switch circuit of claim **1**, wherein a breakdown voltage across the plurality of stacked MOSFET transistors of a selected transistor grouping is n times a breakdown voltage of an individual MOSFET transistor in the selected transistor grouping, wherein n comprises the total number of MOSFET transistors in the selected transistor grouping.

12. The RF switch circuit of claim **1**, wherein RF signals provided to the input ports may swing about a zero reference voltage.

13. The RF switch circuit of claim **7**, wherein the first and second RF input signals have associated input power levels, and wherein increased input power levels can be accommo-

dated by the RF switch circuit by increasing the number of MOSFET transistors per transistor grouping.

14. The RF switch circuit of claim **7**, wherein the first and second RF input signals have associated input power levels, and wherein increased input power levels can be accommodated by the RF switch circuit by varying the physical size of the transistors used in implementing the transistor groupings.

15. A fully integrated RF switch circuit, comprising:

(a) the RF switch circuit as set forth in claim **1**;

(b) a control logic block, coupled to the RF switch circuit, wherein the control logic block outputs the switch control signal (SW) and the inverse switch control signal (SW_); and

(c) a negative voltage generator, coupled to the control logic block, wherein the negative voltage generator receives a positive power supply voltage from an external power supply, and wherein the negative voltage generator outputs a negative power supply voltage.

16. A method of switching RF signals, comprising:

(a) inputting a first RF input signal to a first switch transistor grouping and a first shunt transistor grouping, wherein both the first switch and first shunt transistor groupings comprise a plurality of stacked FETs, each of which has a gate that is insulated from its channel;

(b) inputting a second RF input signal to a second switch transistor grouping and a second shunt transistor grouping, wherein both the second switch and second shunt transistor groupings comprise a plurality of stacked FETs, each of which has a gate that is insulated from its channel;

(c) enabling the first switch transistor grouping while disabling the first shunt transistor grouping, and simultaneously disabling the second switch transistor grouping while enabling the second shunt transistor grouping, thereby passing the first RF input signal and shunting the second RF input signal; and, at exclusively alternative times,

(d) enabling the second switch transistor grouping while disabling the second shunt transistor grouping, and simultaneously disabling the first switch transistor grouping while enabling the first shunt transistor grouping, thereby passing the second RF input signal and shunting the first RF input signal.

17. The method of claim **16**, wherein the RF signals are expected to have a minimum operating frequency Fo, and wherein each FET has a gate capacitance Cg between its gate and its channel, and is coupled to a drive signal via an associated gate resistor Rg, the method further comprising ensuring that a product of Rg times Cg is greater than 1/Fo.

18. The method of claim **17**, wherein the FETs are MOSFETs, and the method further comprises fabricating the switch circuit on a fully insulating sapphire wafer.

19. The method of claim **18**, wherein the method further comprises fabricating the switch circuit on an Ultra-Thin-Silicon ("UTSi") substrate.

20. The method of claim **16**, wherein each FET is coupled to a drive signal via an associated gate resistor Rg having a value of at least about 30 kΩ.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,123,898 B2
APPLICATION NO. : 10/922135
DATED : October 17, 2006
INVENTOR(S) : Burgener et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1, line 10, "Patent No. 6,805,502" should read --Patent No. 6,804,502--.

Signed and Sealed this

Twelfth Day of August, 2008

JON W. DUDAS
Director of the United States Patent and Trademark Office

U.S. DEPARTMENT OF COMMERCE
U.S. PATENT & TRADEMARK OFFICE

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February 01, 2012

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THIS OFFICE OF:

U.S. PATENT: *7,460,852*
ISSUE DATE: *December 02, 2008*

By Authority of the
Under Secretary of Commerce for Intellectual Property
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E. BORNETT
Certifying Officer

US007460852B2

(12) **United States Patent**
Burgener et al.

(10) **Patent No.: US 7,460,852 B2**
(45) **Date of Patent: Dec. 2, 2008**

(54) **SWITCH CIRCUIT AND METHOD OF SWITCHING RADIO FREQUENCY SIGNALS**

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(73) Assignee: **Peregrine Semiconductor Corporation**, San Diego, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **11/582,206**

(22) Filed: **Oct. 16, 2006**

(65) **Prior Publication Data**

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Related U.S. Application Data

(63) Continuation of application No. 10/922,135, filed on Aug. 18, 2004, now Pat. No. 7,123,898, which is a continuation of application No. 10/267,531, filed on Oct. 8, 2002, now Pat. No. 6,804,502.

(60) Provisional application No. 60/328,353, filed on Oct. 10, 2001.

(51) **Int. Cl.**

H04B 1/28	(2006.01)
H01L 26/76	(2006.01)
H04Q 7/20	(2006.01)
H04M 1/00	(2006.01)

(52) **U.S. Cl.** **455/333**; 455/425; 455/550.1; 257/241

(58) **Field of Classification Search** 455/26.1, 455/78, 333, 425, 550.1, 556.1, 560; 257/280–281, 257/341, 472

See application file for complete search history.

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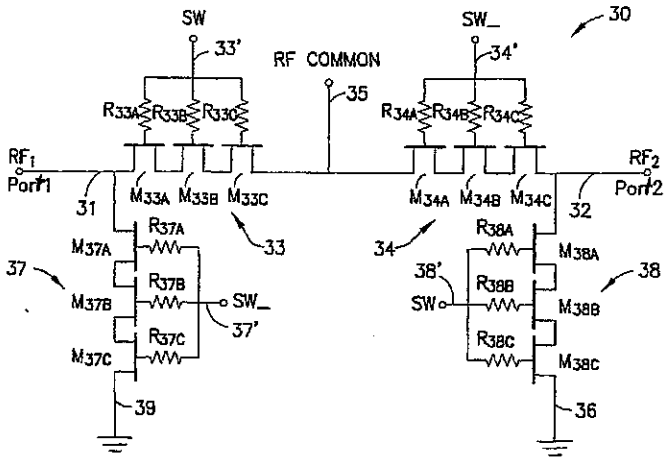
(74) *Attorney, Agent, or Firm*—Jaquez & Associates; Martin J. Jaquez, Esq.

(57) **ABSTRACT**

An RF switch circuit and method for switching RF signals that may be fabricated using common integrated circuit materials such as silicon, particularly using insulating substrate technologies. The RF switch includes switching and shunting transistor groupings to alternatively couple RF input signals to a common RF node, each controlled by a switching control voltage (SW) or its inverse (SW_), which are approximately symmetrical about ground. The transistor groupings each comprise one or more insulating gate FET transistors connected together in a "stacked" series channel configuration, which increases the breakdown voltage across the series connected transistors and improves RF switch compression. A fully integrated RF switch is described including control logic and a negative voltage generator with the RF switch elements. In one embodiment, the fully integrated RF switch includes an oscillator, a charge pump, CMOS logic circuitry, level-shifting and voltage divider circuits, and an RF buffer circuit.

27 Claims, 13 Drawing Sheets



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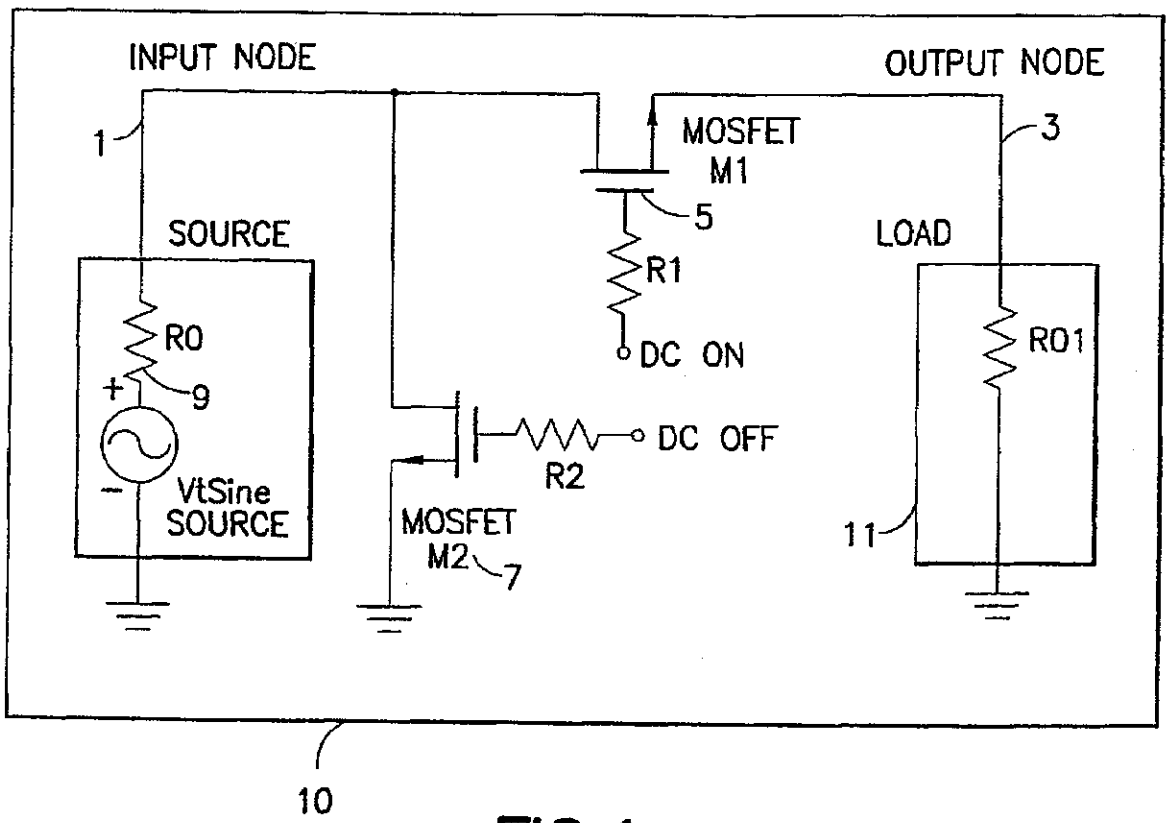

FIG. 1a

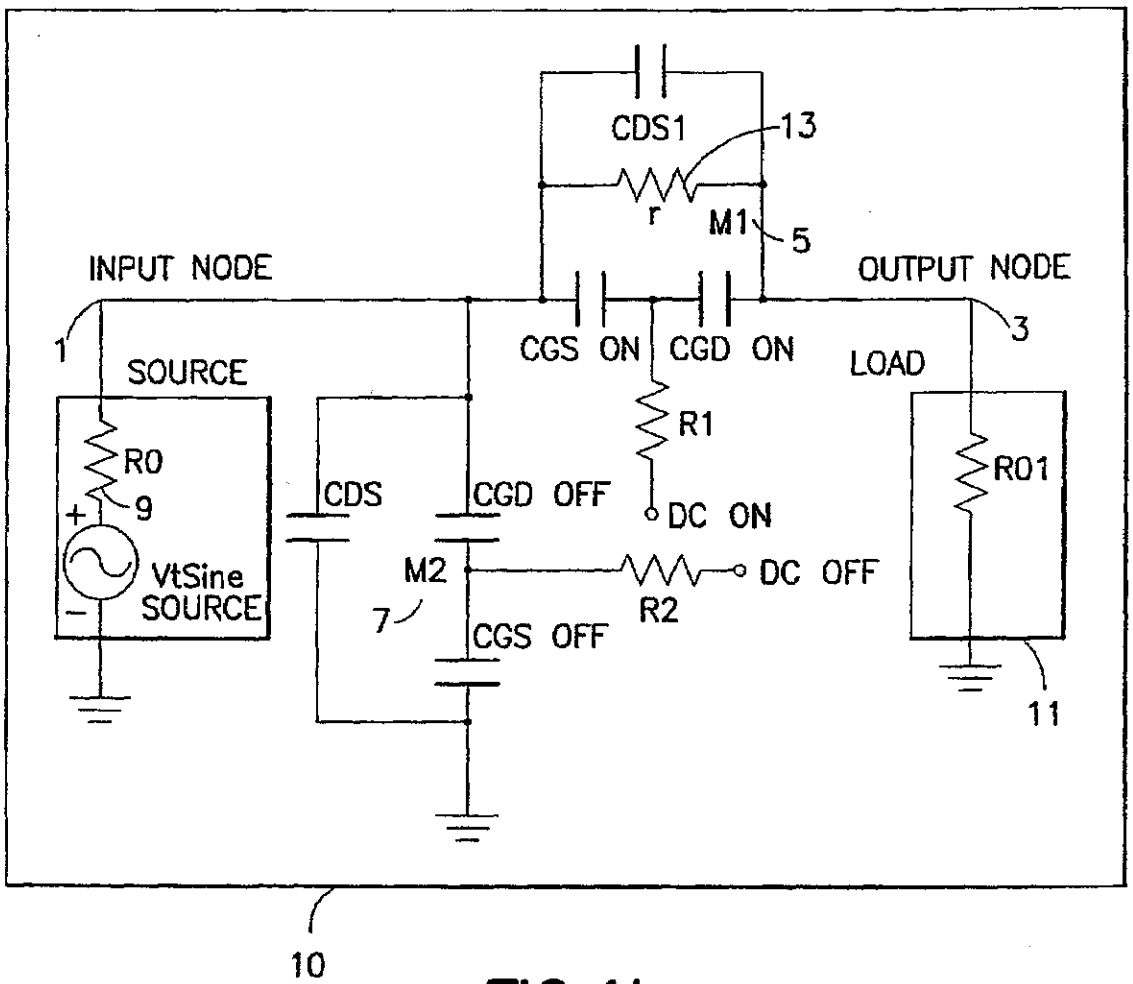

FIG.1b

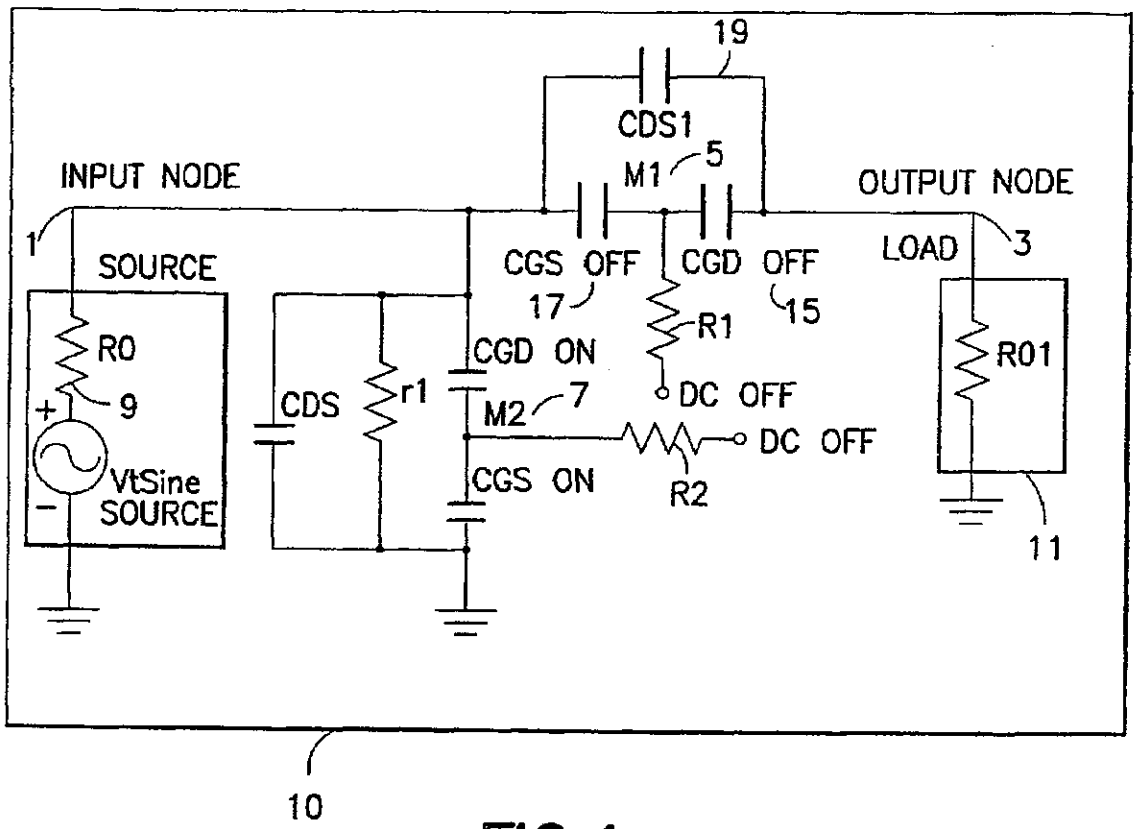

FIG. 1c

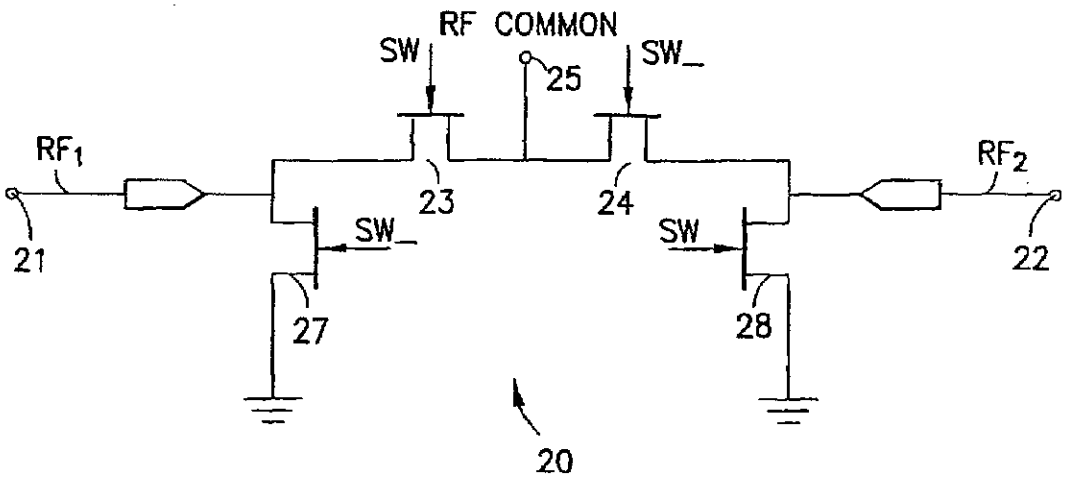

FIG.2

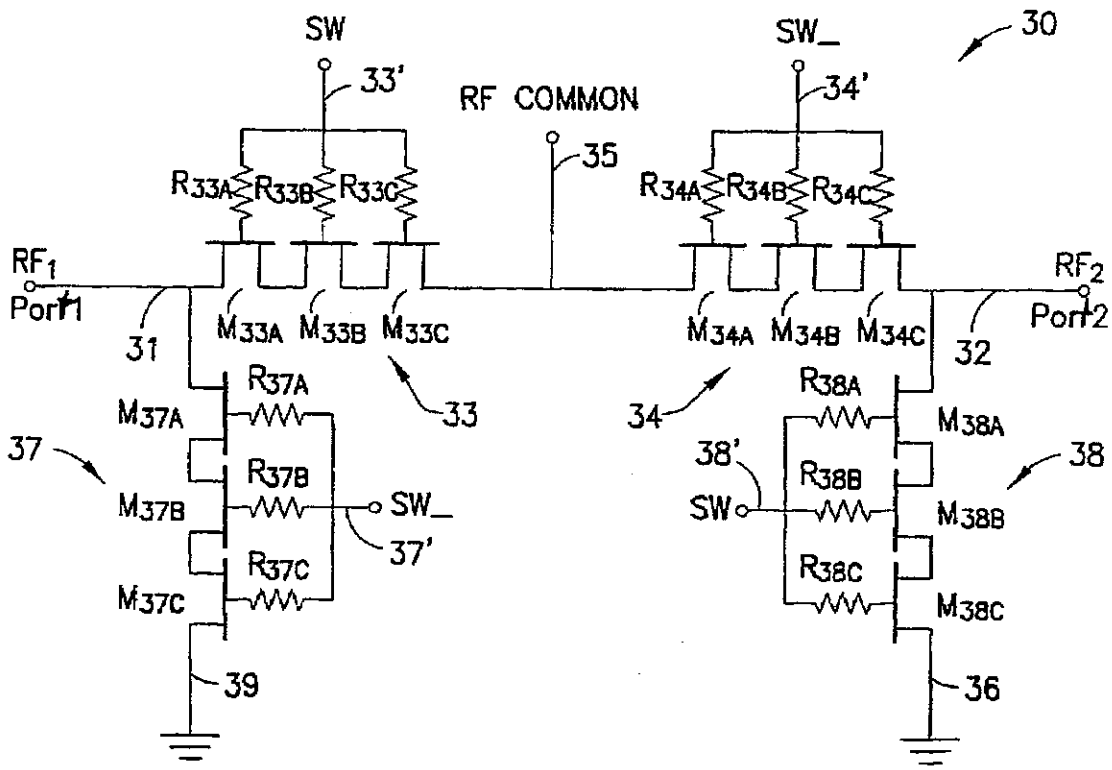

FIG.3